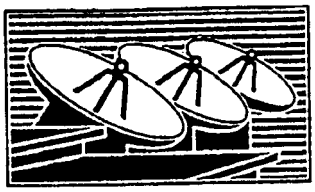


530—STGT—IE312

OPERATION AND MAINTENANCE MANUAL

TEST MODEM

April 1992

National Aeronautics and Space Administration

GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

OPERATION AND MAINTENANCE MANUAL

TEST MODEM

PART NUMBER 7472500 (INTERSTATE ELECTRONICS)

April 1, 1992

Prepared for
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Contract NAS5−33000

Change Information Page

List of Effective Pages	
Page Number	**Issue**
Title	Original
ii	Original
iii and iv	DCN-001
v through xi	Original
xii and xiii	DCN-001
1-1 through 1-42	Original
2-1 through 2-6	Original
3-1 and 3-2	DCN-001
3-3 through 3-11	Original
3-12 through 3-14b	DCN-001
3-15	DCN-001
3-16 through 3-22	Original
4-1 through 4-62	Original
5-1 through 5-22	Original
6-1 through 6-12	Original
7-1 through 7-2	Original
G-1 through G-4	Original

Document History			
Document Number	**Status/Issue**	**Publication Date**	**CCR Number**
530-STGT-IE312	Original	April 1992	
530-STGT-IE312	DCN-001	June 2001	WSC-0750

DCN CONTROL SHEET

Use this control sheet to record the DCN changes to this document.

DCN	DTG	Mon/Yr	Sect.	Initials

TABLE OF CONTENTS

Section 4 — Theory Of Operation

LIST OF ILLUSTRATIONS

LIST OF TABLES

Section 1 – General Description

1–1 Introduction

1 - 1.1 This Level 1 manual is limited to unit operation and maintenance in the installed condition while in local (maintenance) control. Also included is the information necessary to replace and maintain the chassis and all applicable line replaceable units (LRUs) for the Test Modem (TM), part number 7472500.

1 - 1.2 The TM combines with six buy-out test equipment units to form the performance measuring and monitoring system (PMMS) test equipment (PTE). The PTE provides test signals and bit error rate (BER) measuring functions to support pre-service, post-maintenance, and end-to-end test (EET) verification for all S-Band Single Access (SSA), K-Band Single Access (KSA), and Multiple Access (MA) User Services Subsystem (USS) equipment chains.

1 - 1.3 For the purposes of discussion, the TM is considered to consist of two functional entities; the forward demodulator and the return modulator. The forward demodulator is used in the PTE with one of the bit error rate test sets (BERTs), called the forward command channel BERT. The return modulator is used in the PTE with two BERTs (called the return inphase (I) and quadrature (Q) channel BERTs), one Eb/No test set, and two time interval counters (TICs).

1 - 1.4 The TM provides the following essential forward demodulator functions, as required:

a. Provide test data and clock for use by the Modulator/Doppler Predictor (MDP). The data and clock is routed to the MDP through the primary interface.

   (1) Provide local data and clock by commanding and controlling the forward command channel BERTs.

   (2) Use external forward command channel data from the data interface system (DIS).

b. Receive a modulated forward service IF signal from the primary interface.

c. Provide Doppler correction in the forward demodulator, including the capability to:

   (1) Receive Doppler updates (ephemeris data) from the 1553B data bus;

   (2) Maintain a forward model of Doppler compensation and control performed on the forward link.

d. Despread and track the received PN spread signal (one channel only).

e. Provide PN code epoch and clock for range measurement.

f. Demodulate and track the carrier.

g. Recover carrier for Doppler measurement.

h. Support coherent turnaround of the recovered carrier for use by the return modulator.

i. Recover symbol clock and detect symbols.

j. Provide convolutional decoding for recovered symbols.

k. Provide format conversion of recovered data so that the output data stream is NRZ-L.

l. Provide as outputs from the TM to the primary interface the recovered forward command channel data with synchronous clock.

m. For internally generated data (local data), route the recovered forward command channel data and clock to the forward command channel BERT.

n. Provide control of the forward command channel BERT and measure the forward command channel bit error rate (BER).

o. Provide an estimate of the forward command channel bit-power-to-noise ratio (Eb/No).

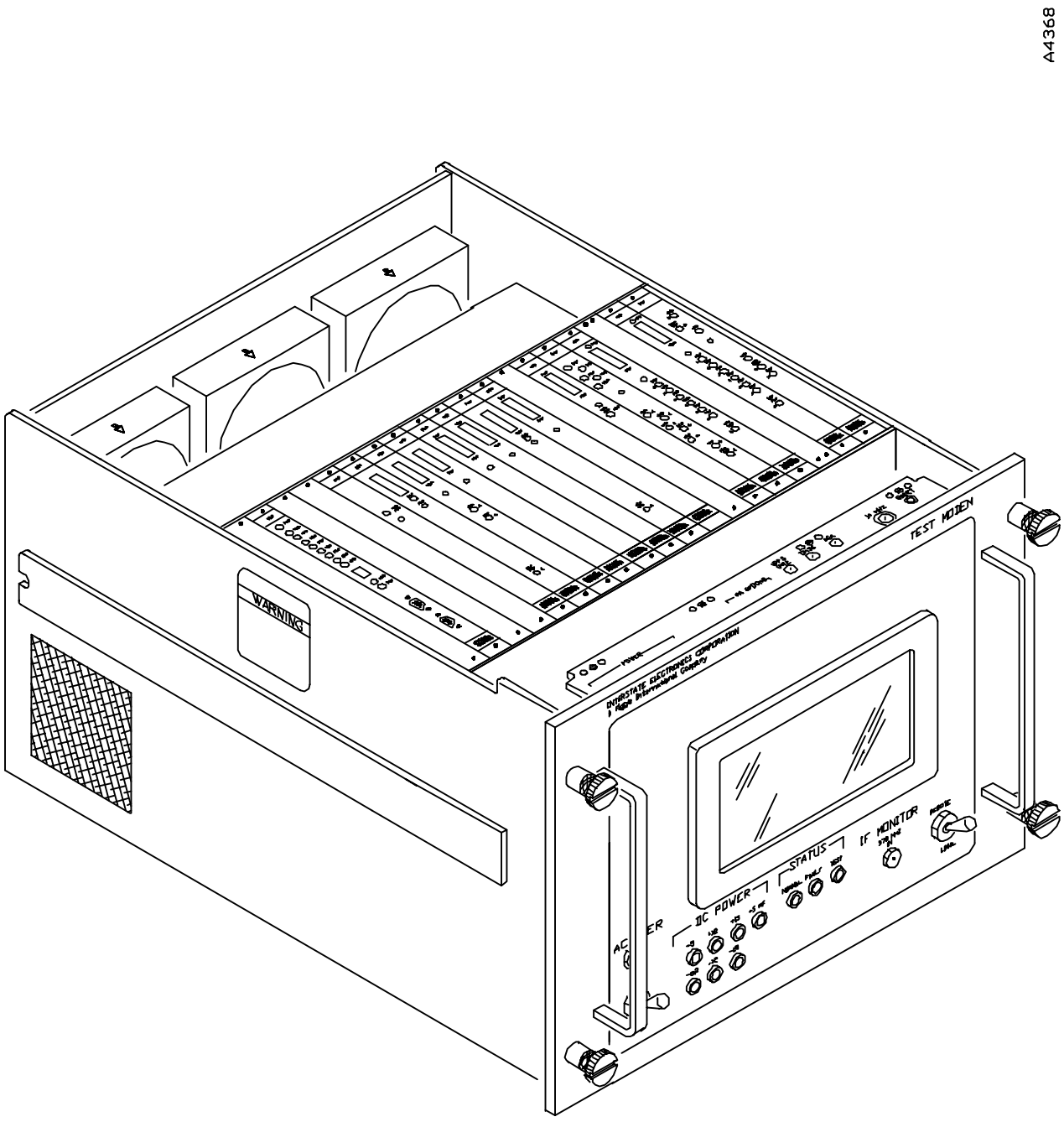


Figure 1 - 1. Test Modem - P/N 7472500

1 - 1.5 The TM provides the following essential return modulator functions, as required:

a. Provide test data and clocks for use by the return modulator.

(1) Provide local NRZ-L format data and clock by commanding and controlling the return I and Q BERTS.

(2) Receive external NRZ-L data and clock from the primary interface and provide appropriate bit synchronization.

(3) Test data and clocks may be local and/or external in that the unit can provide local I data and clock while accepting external Q data and clock, and vice versa.

b. Provide data formatting, convolutional encoding, symbol formatting, and interleaving of return channel data.

c. As commanded, coherently derive a return channel IF carrier from the recovered forward channel IF carrier, or else independently generate a return channel IF carrier.

d. When generating an independent return channel IF carrier, follow a commanded frequency profile using Doppler updates (ephemeris data) from the 1553B data bus.

e. Generate PN codes and clocks.

f. PSK modulate the return channel IF carrier with return channel data and PN codes.

g. Provide the capability to adjust the I to Q channel power ratio.

h. Provide command and control of the Eb/No test set to allow the return channel modulated signal to be set to a commanded carrier-to-noise (C/No) value.

i. Provide the modulated signal as an output to the primary interface at one of two selectable IF output ports (8.5 MHz or 370 MHz).

j. Accept recovered return channel data and clocks from the Integrated Receiver (IR) via the primary interface.

k. Route the recovered return channel data and clocks to the return I and Q channel BERTS and when the data is internally generated (local data), perform BER measurements.

l. For internally generated return channel data, provide data delay measurements by commanding and controlling the TICs.

m. Provide the conditioned baseband data, PN spread if applicable, to the control hardware configuration item (HWCI). Synchronous clock is provided along with data when the data is not PN spread.

n. Provide unmodulated 370 MHz carrier to the control HWCI.

o. Provide the resultant 8.5 MHz test IF signal to the control HWCI.

1 - 1.6 The TM provides the following essential functions which are common to both the forward demodulator and the return modulator, as required:

a. Generate status data, including self-test and fault isolation information, both to the front panel and to the 1553B data bus.

b. Communicate with the primary interface via the MIL-STD-1553B data bus. Table 1-1 lists the various commands and report names and fields used to communicate over the 1553 bus.

c. Communicate with the commercial test equipment (BERTs, Eb/No test set and TICs) via an IEEE-488 data bus.

d. Support maintenance and operation by providing front panel and maintenance panel controls, indicators, and test points, as specified.

1 - 1.7 The information in this manual is presented in seven sections: Section 1, General Description; Section 2, Installation; Section 3, Operation; Section 4, Theory of Operation; Section 5, Maintenance; Section 6, Parts list; and Section 7, Drawings.

1 - 1.8 Section 1 describes the use, capabilities, and technical specifications of the TM. The TM (see figure 1-1; shown with top cover removed) is an integral part of the Second Tracking and Data

Table 1 - 1. TM Commands and Reports

COMMAND	FIELD DEFINITION	REPORT	FIELD DEFINITION
SET STATE	Start checkword Initialization type Initialization data End checkword	MODULATOR CONFIGURATION	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds
GENERAL CONFIGURATION	Start checkword Modulation frequency source End checkword		Service type Setup miscellaneous parameters I/Q power ratio I data format Q data format I encoding Q encoding I symbol format Q symbol format Jitter control
MODULATOR CONFIGURATION	Start checkword Configuration bit map Service type Setup miscellaneous parameters I/Q power ratio I data format Q data format I encoding Q encoding I symbol format Q symbol format Jitter control Single/dual channel modulation I data rate Q data rate Feedback taps Initialize A register value Initialize C register value I data source Q data source Noise on/off C/No setting I BERT PN length Q BERT PN length Nominal IF output frequency		Single/dual channel modulation I data rate Q data rate Feedback taps Initialization A register value Initialization C register value I source Q source Noise on/off C/No setting I BERT PN length Q BERT PN length Nominal IF output frequency KSAR output configuration Service mode Return translation frequency Return modulation IF frequency End checkword

Table 1 - 1. TM Commands and Reports (Continued)

COMMAND	FIELD DEFINITION	REPORT	FIELD DEFINITION
MODULATOR CONFIGURATION (Continued)	KSAR output configuration Service mode Return loop test translation freq Return modulator IF offset freq End checkword	MODULATOR PERFORMANCE	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds Lock status Commands not executed map Commands not accepted map Command not executed error code Command not accepted error code Operating state Delta carrier frequency Ephemeris status End checkword
MODULATION START SERVICE	Start checkword Effective time; hours Effective time; minutes Effective time; seconds End checkword		
DEMOD SPECIFIC CONFIGURATION	Start checkword Configuration bit map Service type Shuttle mode Feedback taps Command channel register A value SSHF PN code rate Forward data rate Test type Forward BERT PN sequence Demod IF offset frequency End checkword	DEMODULATOR CONFIGURATION	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds Service type Feedback taps Command channel register A value Shuttle mode Forward PN modulator configuration SSHF PN code rate Forward data rate Test type Forward BERT PN sequence Forward IF offset frequency Forward translation frequency Demodulation IF offset frequency End checkword
DEMOD COMMON CONFIGURATION	Start checkword Bit map Forward IF offset frequency Forward translation frequency PN modulation configuration End checkword		

Table 1 - 1. TM Commands and Reports (Continued)

COMMAND	FIELD DEFINITION	REPORT	FIELD DEFINITION
DEMOD START ACQUISITION	Start checkword End checkword	DEMODULATOR PERFORMANCE	Start checkword Report time; day Report time; hours
DEMOD START PN MODEL	Start checkword Effective time; hours Effective time; minutes Effective time; seconds End checkword		Report time; minutes Report time; seconds Lock status Commands not executed map Commands not accepted map
START FORWARD BER TEST	Start checkword Forward command word Forward test interval Forward test period End checkword		Command not executed error code Command not accepted error code Operating state
START RETURN BER TEST	Start checkword I command word I test interval I test period Q command word Q test interval Q test period End checkword		Data AGC status 370 IF AGC status Ephemeris status PN model status Eb/No estimate Range delay Integrated Doppler frequency End checkword
MEASURE TIME INTERVAL	Start checkword Command word Trigger setting Trigger level I transmit A Trigger level I receive B Trigger level Q transmit A Trigger level Q receive B End checkword	GENERAL CONFIGURATION	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds Modulator frequency source Confidence test status Online BIT status Local/remote status End checkword

Table 1 - 1. TM Commands and Reports (Continued)

COMMAND	FIELD DEFINITION	REPORT	FIELD DEFINITION
RANGE CHANNEL REACQUISITION	Start checkword End checkword	EXTENDED BIT	Start checkword Completion time; day Completion time; hours Completion time; minutes Completion time;
seconds			MCP test results VME test results TIME test results DMDP test results Demod ASIC test results Signal levels test results PNP test results Correlator tap test results TDIF test results 488 controller test results 488 instruments test results RF loopback test results End checkword
		BER MEASUREMENTS	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds BER test status BERTs error flags Command chnl BER measurement I/Q chnl BER measurement Time interval status Eb/No status Time measurement I Time measurement Q End checkword

Relay Satellite System (TDRSS) Ground Terminal (STGT) USS.

1 - 1.9 This OP-06-1 manual was prepared for the National Aeronautics and Space Administration (NASA) by GE Contract No. NAS5-33000.

1—2 Physical Description

For the purposes of this manual, the major components described are those that are maintained, replaced, or repaired in the installed condition (Level 1 LRUs). Refer to table 1-2 for a listing of the major components (LRUs) of the TM and the illustrations in section 6 for their location. The following information describes the physical characteristics of the chassis and LRUs:

a. Chassis Assembly (TM): EMI-designed to be housed in a standard 19-inch NASA rack. Its physical characteristics are: 12.22 +0.00/-0.03 inches in height, 17.75 inches maximum chassis width (including slides), 24 inches maximum depth, with a total weight more than 74 pounds and not to exceed 85 pounds. The TM makes use of VME double-height printed wiring assemblies (PWAs), RF modules with front panel SMB coaxial and DIN 41612 type M, 60 contact connectors and 4 RF connectors, modular power supplies, and a common baseplate allowing for all internal PWA and RF module (non-RF) interfaces.

b. Power Supply No. 1 (PS1): 4.875” x 7.75” x 12.25” screw-mounted, terminal board wire connections, fan-cooled, 12 pounds maximum, LAMBDA LFQ series power supply.

c. Power Supply No. 2 (PS2): 2.5” x 4.9” x 14.0” screw-mounted, terminal board wire connections, 5.5 pounds maximum, convection-cooled multi-output power supply.

d. Power Supply No. 3 (PS3): 4.9” x 4.03” x 2.78” screw-mounted, hard-wire connections, 12 pounds maximum, 130.0 Vdc power supply.

e. Modem Control Processor (MCP) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, front-panel-mounted LEDs and switches for status/control, and dual front-panel-mounted RS-232/RS-422/RS-485 interface selectable (9-pin) connectors. Utilizes four plug-in sockets to house the latest TM firmware release IC chip set (4); SP7472500-xxx (J21, J23, J25, and J27), where xxx represents the release version. Refer to the label on the inside of the unit top cover for applicable release version.

f. 488 Interface Control (I488) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, and a front-panel-mounted LED.

g. Timing Generator (TIME) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, and front-panel-mounted dual SMB coaxial connectors and a 40-pin test point connector.

h. Test Data Interface (TDIF) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, front-panel-mounted SMB coaxial connectors, and a 40-pin test point connector.

i. Acquisition Processor (ACQR) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, and a front-panel-mounted 40-pin test point connector.

j. PN Processor (PNP) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, and a front-panel-mounted 40-pin test point connector.

k. External Clock Synchronizer (EXCS) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, and a front-panel-mounted 40-pin test point connector.

l. Demod Processor (DMDP) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted,

Table 1 - 2. Major Components

COMPONENT	REF. DES.	FIG. NO.
Test Modem	1	1 - 1
Power Supply No. 1	1A2	6-3-4
Power Supply No. 2	1A3	6-3-3
Modem Control Processor PWA	1A4A1	6-1 - 10
488 Interface Control PWA	1A4A4	6-1 - 9
Timing Generator PWA	1A4A5, 1A4A10	6-1 - 8, 6-1 - 3
Test Data Interface PWA	1A4A6	6-1 - 7
Acquisition Processor PWA	1A4A7	6-1 - 6
PN Processor PWA	1A4A8	6-1 - 5
External Clock Synchronizer PWA	1A4A9	6-1 - 4
Demodulator Processor PWA	1A4A11	6-1 - 2
Demodulator Symbol Synchronizer PWA	1A4A13	6-1 - 11
RF Downconverter No. 2 PWA	1A4A14	6-1 - 12
Synthesizer PWA	1A4A15, 1A4A17	6-1 - 13, 6-1 - 14
Test Modulator PWA	1A4A18	6-1 - 15
Power Supply No. 3	1A5	6-3-2
Touch Panel Display	1A7A1	6-2-7

VME double-height, dual 96-pin DIN 41612 connectors, and a front-panel-mounted 40-pin test point connector. Utilizes two plug-in sockets to house the latest DMDP firmware release IC chip set (2); SP7472110-xxx (J11 and J12), where xxx represents the release version. Refer to the label on the inside of the unit top cover for applicable release version.

m. Demod Symbol Synchronizer (DMSS) PWA: 9.2" x 6.3" printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, a front-panel-mounted SMB coaxial connector and 40-pin test point connector.

n. RF Downconverter No. 2 (RFDC2) PWA: 9.2" x 6.3" printed wiring assembly, screw-mounted, VME double-height, dual 60-pin DIN 41612 type M connectors with four RF connectors each, and front-panel-mounted SMB coaxial connectors (twelve).

o. Synthesizer (SYNTH) PWA: 9.2" x 6.3" printed wiring assembly, screw-mounted, VME double-height, dual 60-pin DIN 41612 type M connectors with four RF connectors each, front-panel-mounted LED, front-panel-mounted SMB coaxial connectors (seven) and 40-pin test point connector.

p. Test Modulator (TMOD) PWA: 9.2" x 6.3" printed wiring assembly, screw-mounted, VME double-height, dual 60-pin DIN 41612 type M connectors with four RF connectors each, and front-panel-mounted SMB coaxial connectors (six).

q. Front Panel Touch Display: 9.0" x 12.5" x 3.74" interactive alphanumeric display with an Amp Mate-N-Lok 1-480270-0 power connector, a 3M 3399-6040 parallel input connector, a 3M 3399-6026 parallel output connector, and a 25 pin male D-type serial connector.

1–3 Functional Description

This paragraph provides a brief functional description of the chassis and each Level 1 LRU. Items covered include the overall function of the chassis unit as a whole and then each LRU as it applies to pertinent input/output signals.

1–3.1 TM Chassis Assembly

The PTE (the TM and associated equipment) is used interchangeably in the KSA low data rate equipment configurations, SSA equipment configurations, or MA receiver/transmit equipment configurations. Figure 1-2 shows the configuration of components that make-up the PTE. PTE interfaces with the SSA, KSA, and MA control HWCIs in the SSA, KSA, and MA portions of the USS, respectively. Furthermore, the PTE is utilized in the STGT Electronics System Test Set (refer to STGT Electronics System Test Set Level 1 operation and maintenance manual; 530-STGT-IE313 for further information within this configuration). Figure 1-3 shows the SSA, SSH, and MA receive/transmit interface configurations and figure 1-4 shows the KSA low data rate and KSH interface configuration. Figures 1-5, 1-6, and 1-7 show the simplified signal flows for the KSA, SSA, and MA, respectively.

1–3.2 Power Supply No. 1

PS1 accepts the 120-Vac site-supplied power and outputs regulated +5.0 Vdc, +5.0 RF Vdc, and +/-15.0 Vdc source power for circuits throughout the TM.

1–3.3 Power Supply No. 2

PS2 accepts the 120-Vac site-supplied power and outputs regulated -5.2 Vdc and +/-12.0 Vdc source power for circuits throughout the TM.

1–3.4 Power Supply No. 3

PS3 accepts the 120-Vac site-supplied power and outputs regulated +130.0 Vdc to the touch panel display.

1–3.5 Modem Control Processor PWA

1-3.5.1 MCP Functions - The MCP provides the required computations, scheduling of events,

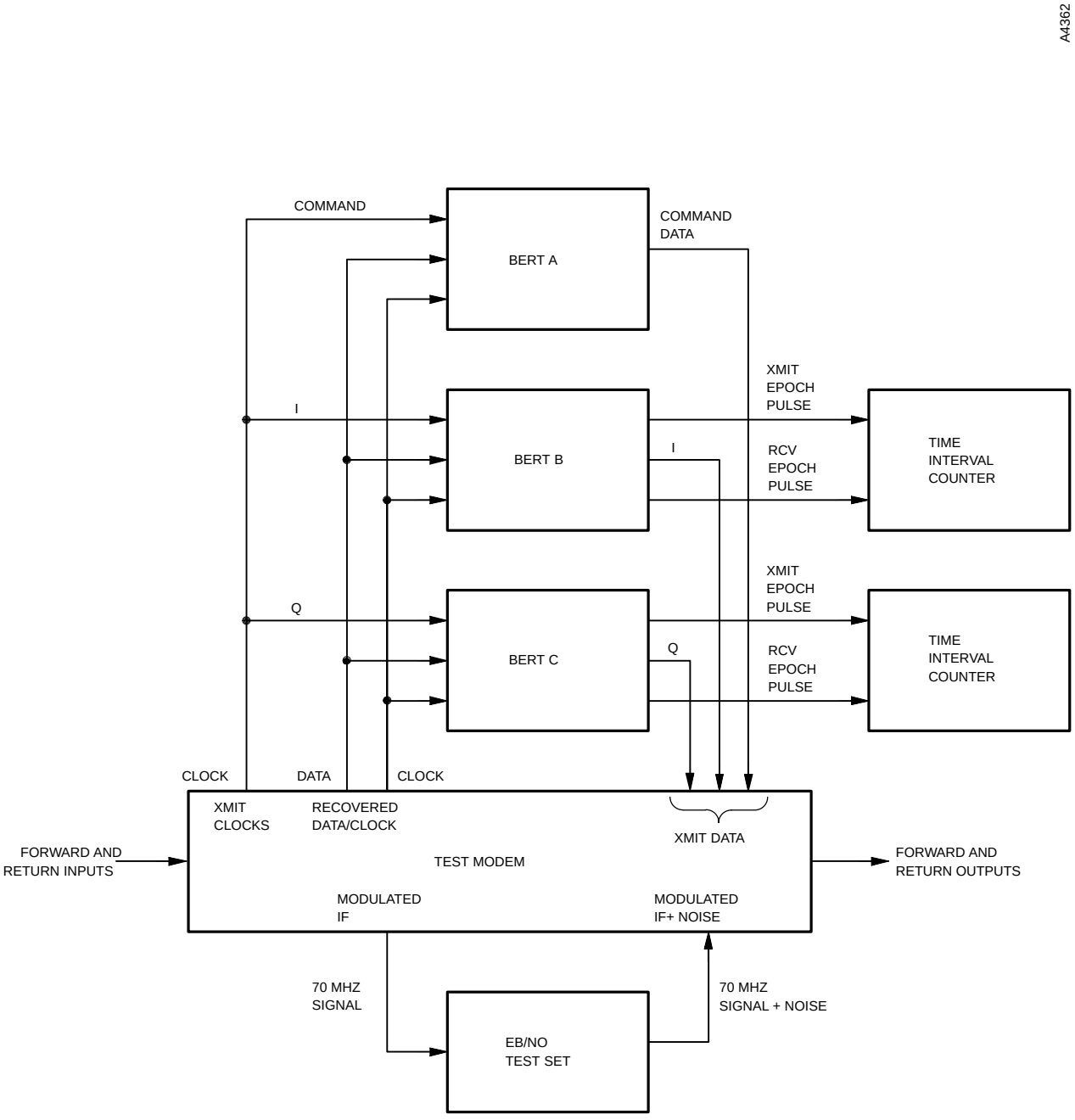
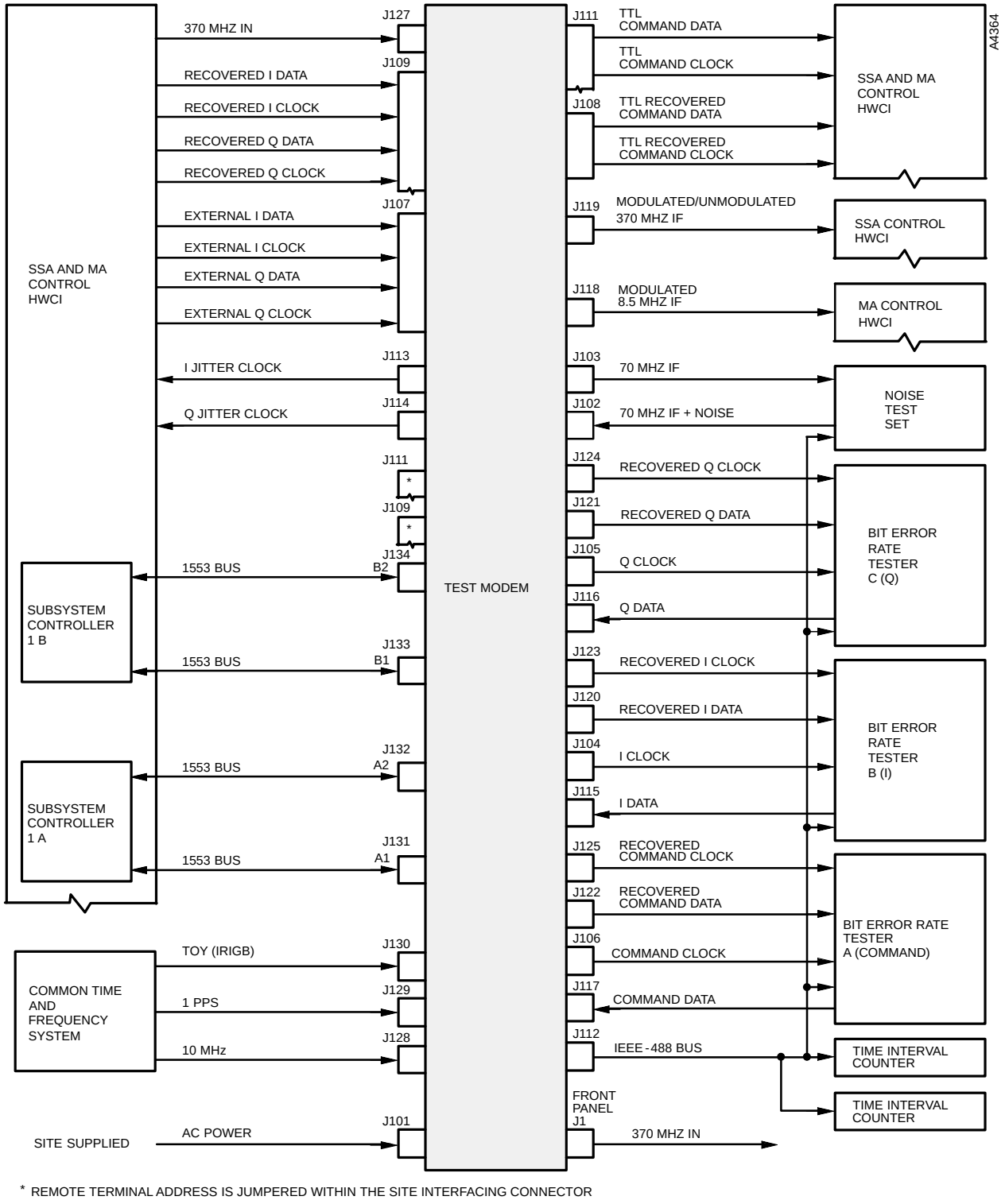
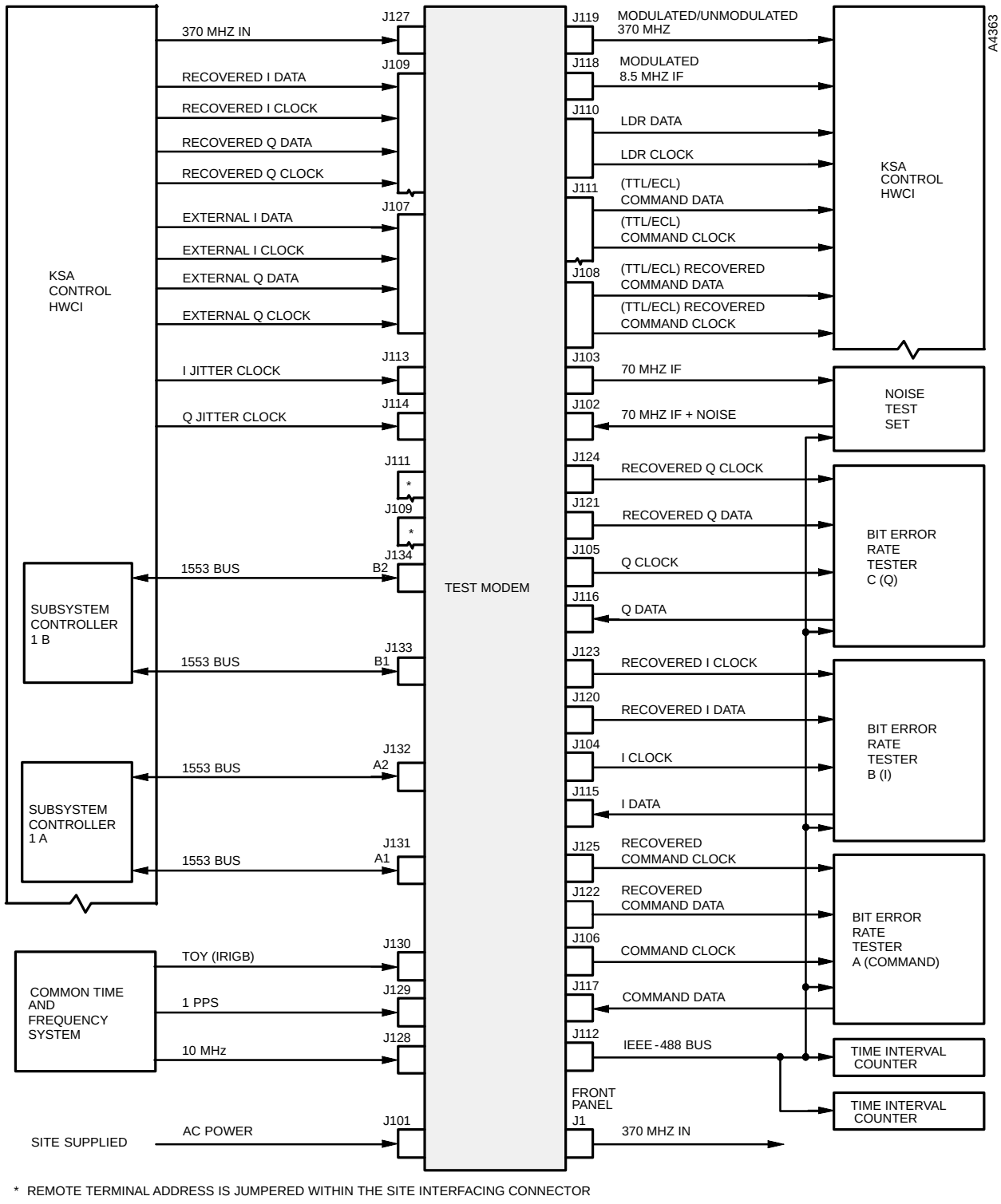


Figure 1 - 2. Test Modem and Associated Equipment (PTE) Configuration



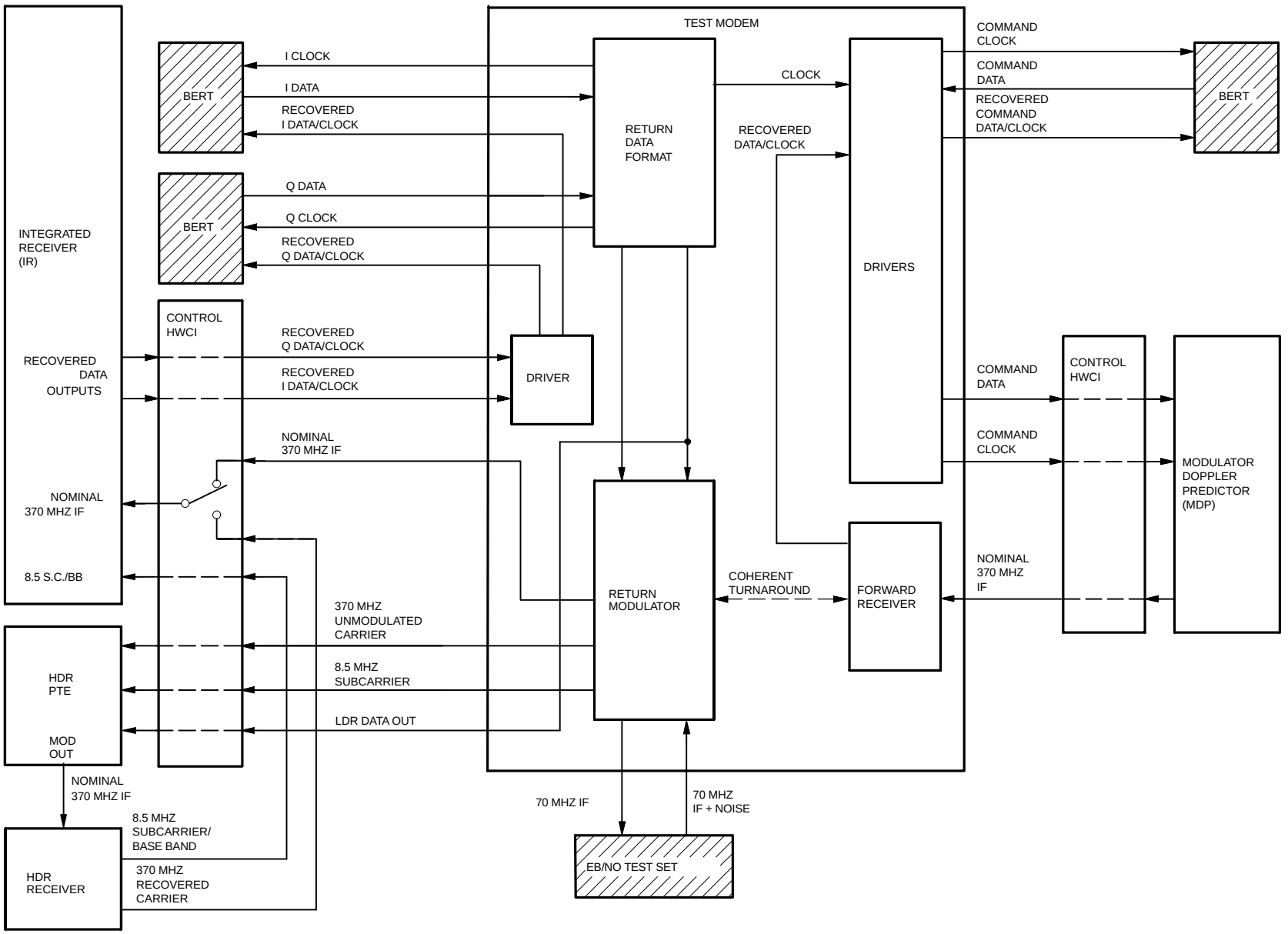
* REMOTE TERMINAL ADDRESS IS JUMPERED WITHIN THE SITE INTERFACING CONNECTOR

Figure 1 - 3. Test Modem Interfaces for SSA, SSH, and MA Receiver/Transmit Equipment Configuration



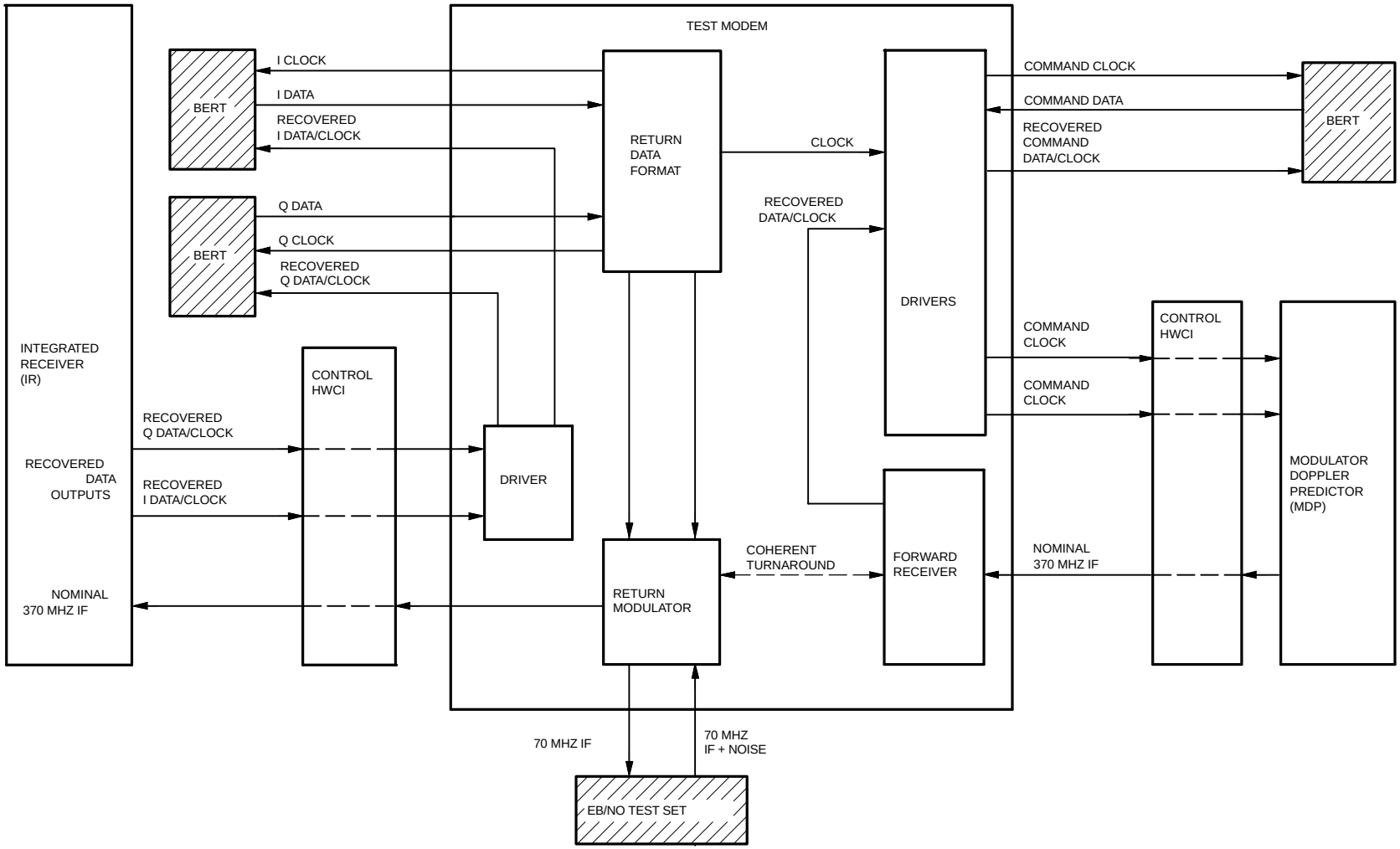
* REMOTE TERMINAL ADDRESS IS JUMPERED WITHIN THE SITE INTERFACING CONNECTOR

Figure 1 - 4. Test Modem Interfaces for KSA Low Data Rate and KSH Equipment Configuration



NOTE: SHADED BLOCKS ARE COMMERCIALLY AVAILABLE EQUIPMENTS.

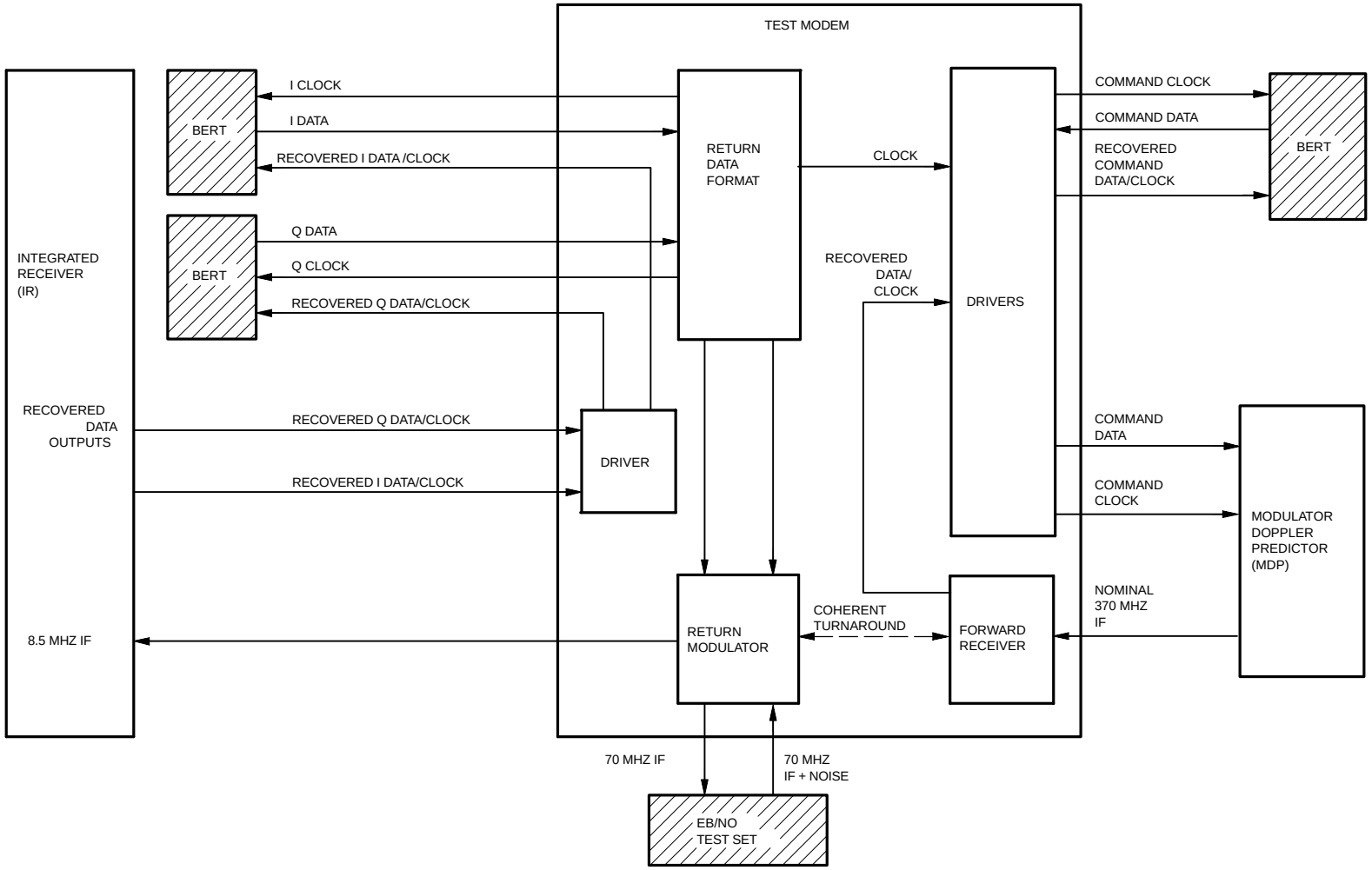
Figure 1 - 5. KSA Simplified Signal Flow



NOTE: SHADED BLOCKS ARE COMMERCIALLY AVAILABLE EQUIPMENTS

Figure 1 - 6. SSA Simplified Signal Flow

A4366



NOTE: SHADED BLOCKS ARE COMMERCIALLY AVAILABLE EQUIPMENTS.

A4365

Figure 1 - 7. MA Simplified Signal Flow

and overall control of TM operations via the VMEbus. The MCP provides the following:

a. A 68030 central processing unit (CPU) operating at 25 MHz.

b. Capability of up to 5 mega-instructions per second (MIPS) through the 1-Mbyte onboard static random access memory (SRAM) and the on-chip cache.

c. Two 68561 multiprotocol communications controllers (MPCCs) for serial I/O (RS-232 compatible interface with one channel-selectable RS-232/RS-422/RS-485).

d. Two parallel interface and timer (PI/T) devices for local control, interrupt level control, and timer functions.

e. Two 68153 bus interrupter modules (BIMs) for all local interrupts.

1 - 3.5.2 MCP Interfaces - The MCP interfaces with the following:

a. PNP: (via VMEbus) MCP provides PN acquisition control, tracking, and NCO control.

b. TIME: (via VMEbus) MCP provides control of the 1553 TM interface, IRIG-B data, NCO, and VMEbus access to various timing, voltage, temperature and epoch measurements.

c. Front panel to control the interactive touch-panel display.

d. ACQR: (via VMEbus) MCP provides configuration/operation control and accepts peak search detect data.

e. DMDP: (via VMEbus) MCP provides configuration/operation control and accepts status data.

f. TDIF: (via VMEbus) MCP provides test modulator configuration/operation control and accepts status data.

g. EXCS: (via VMEbus) MCP provides test decoding configuration/operation control and accepts status data.

h. I488: (via VMEbus) MCP provides configuration/operation control and accepts status and test equipment data

1–3.6 488 Interface Control PWA

I488 provides a VMEbus interface to the IEEE-488 bus interface capability. The I488 interfaces with the following:

a. IEEE-488 bus interface to external test equipment.

b. MCP: (via the VMEbus) I488 accepts configuration/operation control data and provides status and test equipment data via the IEEE-488 bus interface.

1–3.7 Timing Generator PWA

1 - 3.7.1 TIME Functions - TIME provides the following functions: alignment of internal timing with CTFS supplied 1 PPS, time-of-year (TOY) data from IRIGB, timing and epoch interrupts, time transfer measurement (epoch count), provides communications with the VMEbus via a MIL-STD-1553 interface, control/status interface between RF PWAs and VMEbus, two numerically controlled oscillators (NCOs) per PWA, power source measurements, and front-panel interface.

1 - 3.7.2 TIME1 Interfaces - TIME1 interfaces with the following:

a. Time-of-year (seconds, minutes, hours, and days) information to the VMEbus from the input serial IRIG-B data.

b. A controlled 1553 interface with the VMEbus.

c. PNP: TIME1 provides timing signals and accepts PN code epochs.

d. Control/status communication between the RF modules, SYNTH, and the VMEbus.

e. Timing and epoch interrupts to the VMEbus from the 1 PPS, epoch, and 50-MHz signals and accepts masking of any or all of these interrupts. An epoch count to the VMEbus. The epoch count is defined as the number of 10-MHz clocks between the 1 PPS and the epoch mark.

f. An NCO output to both SYNTH1 and SYNTH2 which is VMEbus controlled.

g. Output digitized voltage measurements of various power sources to the VMEbus upon command.

h. A register that is capable of being observed at test points on the P3 connector and is controllable by the VMEbus. A driver register that interfaces the VMEbus and P2 connector.

i. DMSS and DMDP: TIME1 provides various timing signals.

1 - 3.7.3 TIME2 Interfaces - TIME2 interfaces with the following:

a. A controlled 1553 bus interface with the VMEbus.

b. SYNTH2: TIME2 accepts status information.

c. Two NCO outputs and a 50-MHz clock to TDIF.

1–3.8 Test Data Interface PWA

1 - 3.8.1 TDIF Functions - TDIF provides the applicable STGT return service test signal data conditioning, encoding, and PN modulation required for the selected test configuration. The TDIF supports the following configurational modes: SSAF, MAF, KSAF, SSHF, and KSHF.

1 - 3.8.2 TDIF Interfaces - TDIF interfaces with the following:

a. TMOD: TDIF provides I channel data, Q channel data, and signal modulation control.

b. TIME2: TDIF accepts PN code NCO 1 & 2.

c. TIME1: TDIF accepts a 1-kHz timing signal.

d. EXCS: TDIF accepts two phased-lock loop I/Q data clocks for circuit synchronization and data clocking depending upon configurational setup.

e. MCP: (via the VMEbus) TDIF accepts configuration/operation control data and provides status data.

f. External BERT equipment to supply data clock, recovered channel data, and accept test channel data. Also outputs low data rate data/clock during high-data rate configurations. Accepts external I/Q data and jitter clocks from control HWCI; depending upon configurational setup.

1–3.9 Acquisition Processor PWA

1 - 3.9.1 ACQR Functions - ACQR provides a VMEbus interface and I/Q correlator data coherent/noncoherent combining processes. These processes provide correlation peak information to the MCP (via the VMEbus) to steer the PN code acquisition and tracking function.

1 - 3.9.2 ACQR Interfaces - ACQR interfaces with the following:

a. DMSS: ACQR accepts I and Q correlator data.

b. PNP: ACQR accepts timing and control signals. These signals direct the data flow through the ACQR, particularly the number of coherent and noncoherent combines intervals and/or subintervals.

c. MCP: (via the VMEbus) ACQR accepts configuration/operation control data and provides peak detect data.

1–3.10 PN Processor PWA

1 - 3.10.1 PNP Functions - PNP provides a VMEbus interface and generates two I and Q PN code strings for the acquisition and tracking of spread spectrum TDRSS forward service test signals.

1 - 3.10.2 PNP Interfaces - PNP interfaces with the following:

a. DMSS: PNP provides PN data and associated clocks.

b. ACQR: PNP provides timing and control signals. These signals direct the data flow through the ACQR, particularly the number of coherent and noncoherent combines intervals and/or subintervals.

c. MCP: (via the VMEbus) PNP accepts configuration/operation control data.

d. TIME1: PNP accepts timing signals and outputs PN code epochs.

1–3.11 External Clock Synchronizer PWA

1 - 3.11.1 EXCS Functions - EXCS provides a VMEbus interface, two phased-lock loops that generate I and Q data clocks, interfacing circuitry for selection of externally input I and Q data clocks, differential decoding, and Shuttle decoding of symbol data from the DMSS.

1 - 3.11.2 EXCS Interfaces - EXCS interfaces with the following:

a. DMSS: EXCS accepts symbol data and clock for command data recovery.

b. TIME2: EXCS accepts a 50-MHz timing signal.

c. TIME1: EXCS accepts a 1-kHz timing signal.

d. TDIF: EXCS provides two phased-lock loop I/Q data clocks or external I/Q data clocks for circuit synchronization and data clocking depending upon configurational setup.

e. MCP: (via the VMEbus) EXCS accepts configuration/operation control data and provides status data.

f. External Command BERT equipment: EXCS supplies recovered data clock and recovered command channel data. Accepts external I/Q clocks and supplies recovered command channel data and clock with the control HWCI; depending upon configurational setup.

1–3.12 Demodulator Processor PWA

1 - 3.12.1 DMDP Functions - DMDP consists of a digital signal processor (DSP), a fast fourier transform (FFT) controller, and the associated hardware to perform the following functions:

a. Communicate control, configuration, and status information with the MCP via the VMEbus.

b. Control signal tracking loops as required by the configuration. This function uses an FFT process to acquire the carrier, and second- and third-order digital PLLs to track it. Control information is sent to, and status and data received from the DMSS via the TMS bus.

c. Provide non-coherent automatic gain control (AGC) and dc-bias compensation to maintain proper signal input levels from the RF section of the unit to the digital processing section.

1 - 3.12.2 DMDP Interfaces - DMDP interfaces with the following:

a. DMSS: DMDP provides signal tracking loop control (via TMS bus) and accepts FFT I/Q data.

b. MCP: (via the VMEbus) DMDP accepts configuration/operation control data and provides status data.

c. RFDC: DMDP provides AGC and I/Q offset control.

1–3.13 Demodulator/Symbol Synchronizer PWA

1 - 3.13.1 DMSS Functions - DMSS provides a TMS bus interface, I and Q data filtering from the RFDC, two 2-bit variable length correlators, symbol/data recovery processes, and a loop-back 8.5-MHz carrier LO signal.

1 - 3.13.2 DMSS Interfaces - DMSS interfaces with the following:

a. DMDP: DMSS provides a controlled TMS bus interface and FFT I/Q data.

b. SYNTH1: DMSS accepts a 70-MHz clock for the Demod chip NCO.

c. RFDC2: DMSS accepts digitized I, Q, and BB components of the processed forward service test IF signal and provides an 8.5-MHz LO signal and sample clock for proper downconversion and digitization.

d. TIME1: DMSS accepts various timing signals.

e. PNP: DMSS accepts PN data and associated clocks.

f. ACQR: DMSS provides I and Q correlator data.

g. EXCS: DMSS provides symbol data and clock for command data recovery.

1–3.14 RF Downconverter No. 2

1 - 3.14.1 RFDC2 Functions - RFDC2 provides RF downconversion and digitization of various STGT return service IF signals. It also accepts control from and provides status to the TIME PWA.

1 - 3.14.2 RFDC2 Interfaces - RFDC2 interfaces with the following:

a. DMSS: RFDC2 provides digitized I_I and Q_I components of the processed LDR return service or digitized Q BB components from the HDR data. Also, accepts an 8.5-MHz LO signal and sample clock for proper downconversion and digitization.

b. SYNTH1: RFDC2 accepts the 300-MHz LO and 61.5-MHz LO downconversion signals and a 70-MHz test signal.

c. TIME1: RFDC2 accepts control signals for signal selection.

d. External input to accept the 370-MHz IF forward service signal.

e. DMDP: RFDC2 accepts AGC and I/Q offset control.

1–3.15 Synthesizer PWA

1 - 3.15.1 SYNTH Functions - SYNTH provides various fixed and variable timing signals used for RF downconversion of the STGT forward service test IF signals (SYNTH1) and upconversion of the return service test IF signals (SYNTH2). Status of the resident PLLs are provided to MCP via their respective TIME PWAs.

1 - 3.15.2 SYNTH1 Interfaces - SYNTH1 interfaces with the following:

a. RFDC2: SYNTH1 provides the 300-MHz LO and 61.5-MHz LO downconversion signals and a 70-MHz test signal.

b. External input to accept a 10-MHz reference timing signal.

c. SYNTH2: SYNTH1 provides a 10-MHz reference timing signal.

d. TIME1: SYNTH1 provides a 50-MHz clock and PLL status signals and accepts a 20-MHz/8.5-MHz (depending upon configuration) base timing signal. Also, SYNTH1 accepts an MA select signal for output signal selection.

e. DMSS: SYNTH1 provides a 70-MHz clock for the Demod chip NCO.

1 - 3.15.3 SYNTH2 Interfaces - SYNTH2 interfaces with the following:

a. TMOD: SYNTH2 provides the 300-MHz LO and 61.5-MHz LO downconversion signals and a 70-MHz test signal.

b. TIME1: SYNTH2 accepts a 20-MHz/8.5-MHz NCO base timing signal and TIME2 to provide PLL status signals.

c. SYNTH1: SYNTH2 accepts a 10-MHz reference timing signal.

1–3.16 Test Modulator PWA

1 - 3.16.1 TMOD Functions - TMOD provides QPSK/UQPSK modulation of the I and Q input data streams and upconverts the modulated

70-MHz IF signal to 370-MHz IF for output or downconverts it to an 8.5-MHz IF output. Automatic level control is provided by TMOD to both the modulated and unmodulated 370-MHz IF outputs.

1 - 3.16.2 TMOD Interfaces - TMOD interfaces with the following:

a. TDIF: TMOD accepts Q channel data, I channel data, and signal processing control.

b. SYNTH2: TMOD accepts the 300-MHz LO, 70-MHz LO, and variable 61.5-MHz LO signal processing frequencies.

c. TIME1: TMOD provides modulated and unmodulated ALC signals for conversion and monitoring.

1–3.17 Touch Panel Display

The touch panel display is an interactive terminal using the Argus alphanumeric display module to display messages, and a touch-input infrared switch matrix to record user responses. The Argus alphanumeric display uses dc-excited plasma technology to display characters in a 5x7 dot format with underline and forward cursor capability. The switch matrix is an X-Y array of active locations formed by intersecting beams of infrared light generated by LED elements. When a set of X-Y beams is broken, a switch closure is detected and the switch position is transmitted to the MCP. Each active area (approximately 0.2x0.2 inches) is centrally located between two horizontal display character locations. Thus, there are 240 active switch locations arranged in 12 rows of 20 columns.

1–4 Condensed Data

As applicable, refer to the following tables and figure for TM Level 1 maintenance:

a. Table 1-3, Electrical Characteristics; this table lists all input/output electrical characteristics of the TM chassis and Level 1 LRUs. Figure 1-8 shows the relationships between the differential clock and data.

b. Table 1-4, NASA Drawings; this table lists all TM chassis and Level 1 LRU technical illustrations contained in sections 1 and 5 that have NASA drawing numbers assigned.

c. Table 1-5, Environmental Requirements; this table lists environmental conditions that the TM will not suffer permanent degradation or damage when subjected to.

d. Table 1-6, Equipment Required, but Not Supplied; this table lists all equipment required for TM Level 1 maintenance, but not supplied with the unit.

e. Table 1-7, Consumables; this table lists all required consumables for TM Level 1 maintenance.

1–5 Special Tools and Test Equipment

Table 1-8 lists and describes the special tools and test equipment required to maintain the TM only in the installed condition (Level 1 maintenance). All chassis-installed maintenance is performed using standard handtools. If any of the listed items are not available, equivalent part numbers may be used. The TM is supported, as part of the USS, by the maintenance test group (MTG). The MTG provides control of test configuration, injection of test stimuli, measurements of equipment responses to stimuli, and displays results in a manner to permit failure localization.

Table 1 - 3. Electrical Characteristics	
PARAMETER	DESCRIPTON
PHYSICAL CHARACTERISTICS	
Panel height	12.22, +0.00/-0.03 inches
Panel width	18.97, +0.00/-0.03 inches
Chassis depth	24 inches, maximum
Chassis width	17.75 inches, maximum (including slides)
Weight	85 pounds, maximum
POWER REQUIREMENTS	
Voltage	120 Vac; +/- 10% voltage regulation, single phase
Frequency	60 +/-3 Hz
Transients	+/- 15% of nominal voltage; surge for less than 0.5 seconds
Power consumption	700 watts, maximum
Panel connectors	Rear panel: 1A1J101, AC connector
370-MHz INPUT IF	
Nominal Frequency	370 MHz
Reference Bandwidth	30 MHz, centered about 370 MHz
VSWR from Control HWCI	Less than 1.3:1 over the reference bandwidth
Nominal Impedance	50 ohms
Signal plus noise level in the reference bandwidth for SSAF, SSHF, and MAF	
EET	-25.5 dBm, +/-6 dBm in a 50 MHz reference bandwidth centered about 370 MHz
Internal loopback	-29 dBm, +/-9 dBm with a C/No greater than 100 dB-Hz
Spurious signals	The total RSS value of all spurious signals within a 50 MHz bandwidth centered about 370 MHz will be -30 dBc, maximum; no single spurious signal will exceed -40 dBc

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
370 - MHz INPUT IF (Continued)	
Signal plus noise level in the reference bandwidth for KSAF and KSHF	
EET	- 25.5 dBm, +/ - 6 dBm in a 100 MHz reference bandwidth centered about 370 MHz
Internal loopback	- 29 dBm, +/ - 9 dBm with a C/No greater than 100 dB - Hz
Spurious signals	The total RSS value of all spurious signals within a 100 MHz bandwidth centered about 370 MHz will be - 30 dBc, maximum; no single spurious signal will exceed - 40 dBc
Panel connectors	Rear panel: 1A1J127, SMA female
CTFS INPUTS	
10 MHz	
Frequency	10 MHz
Waveform	Sinusoidal
Impedance	50 ohms
Level	+11 dBm +/ - 2 dB into 50 ohms
Single Sideband Phase Noise	Better than - 140 dBc for 1 kHz offset measured in a 1 Hz bandwidth
Accuracy	+/ - 4 x 10^{-12}
Stability	+/ - 8.5 x 10^{-13} long term (100 seconds) +/ - 5 x 10^{-12} short term (1 second)
Input VSWR	Better than 1.3:1 in a bandwidth from 9.5 MHz to 10.5 MHz
Panel connectors	Rear panel: 1A1J128, SMA female

Table 1 - 3. Electrical Characteristics (Continued)	
PARAMETER	DESCRIPTON
CTFS INPUTS (Continued)	
1 PPS	
Frequency	1 Hz
Waveform	Single ended, rectangular pulse
Impedance	50 ohms
Level	TTL levels
Pulse Width, t_w	100 microseconds, +/-0.1%
Rise and Fall Times	< 10 nanoseconds
Jitter	< 2 nanoseconds
Accuracy	< +/- 25 nanoseconds referenced to the CTFS master epoch
Panel connectors	Rear panel: 1A1J129, SMA female
Time of Year (TOY)	
Signal Format	IRIG-B level shift
Impedance	50 ohms, nominal
Levels	TTL into 50 ohms
Panel connectors	Rear panel: 1A1J130, SMA female
1553 BUS	
Description	The TM communicates, on one of four 1553 buses, with the primary interface via a MIL-STD-1553B Digital Time Division Command Response Multiplex Data Bus with the TM configured as a remote terminal. Refer to ICD STGT-HE-06-2; GES-STGT-0004 for interface configuration and control information.
Mode	Single channel, redundant

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
1553 BUS (Continued)	
Coupling	Transformer coupled
Remote terminal address (RTA)	The TM RTA for the A side bus is accommodated via the primary interface connector J109. The TM RTA for the B side bus is accommodated via the primary interface connector J111. The TM provides internal pull ups for the input signals. See table 4-1.
Parity	Odd
Panel connectors	Rear panel: 1A1J131, 1A1J132, 1A1J133, and 1A1J134 Twinax (threaded)
IEEE-488 BUS	
Description	The TM utilizes a GPIB-1014-2 which is a high performance IEEE-488 interface for the VMEbus with a direct memory access bus transfer
Rate	500 kilobytes per second, maximum
Panel connector	Rear panel: 1A1J112, 24 pin Cinch
I/Q SIMULATED USER RETURN DATA AND CLOCK SIGNALS	
Data format	NRZ
Data rate	100 bps to 6 Mbps on I and Q channels; 100 bps to 12 Mbps on I channel for single channel user
Clock rate	Same as data rate and synchronous with data
Signal level (clock or data)	Differential (A) to (B) voltage, 400 mV, minimum (see figure 1 - 8)
Signal type	Complementary balanced differential TTL
Nominal source impedance	Less than 10 ohms
Clock asymmetry	50 +/-5%, maximum

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
I/Q SIMULATED USER RETURN DATA AND CLOCK SIGNALS (Continued)	
Clock asymmetry	50 +/-5%, maximum
Time skew (data to clock)	(A) to (A) and (B) to (B), 25 % of a bit period, maximum
Time skew (data or clock)	(A) to (B) 6.5 nanoseconds, maximum
Transition time, 20% to 80% differential (data and clock)	18 nanoseconds, maximum
Output impedance	100 ohms +/-2% line-to-line for each differential signal pair
Panel Connectors	Rear panel: 1A1J107, 15 pin male D type
PTE BASEBAND DATA AND CLOCK INPUT SIGNALS	
Data format	NRZ
Data rate	SSA: 100 bps to 6 Mbps on I and Q channels; 100 bps to 12 Mbps on I channel for single channel user KSA: 1 kbps to 6 Mbps on I and Q channels; 1 kbps to 12 Mbps on I channel for single channel user MA: 100 bps to 50 kbps on I and Q channels; 100 bps to 50 kbps on I channel for single channel user
Clock rate	Same as data rate and synchronous with data
Source impedance	Less than 10 ohms
Signal level	RS-422A (I and Q channels may be independent (asynchronous) with respect to each other
Data type	Complimentary balanced differential TTL
Input impedance	100 ohms +/-2% line-to-line for each differential pair

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
PTE BASEBAND DATA AND CLOCK INPUT SIGNALS (Continued)	
Panel connectors	Rear panel: 1A1J109, 15 pin male D type
PTE BASEBAND COMMAND DATA AND CLOCK OUTPUT SIGNALS	
Data format	NRZ
Data rate	SSA: 100 bps - 300 kbps KSA: 1 kbps - 25 Mbps MA: 100 bps - 10 kbps
Clock rate	Same as data rate and synchronous with data
Signal type	Similar to RS-422A (see figure 1 - 8)
Data type	Complementary balanced differential TTL
Clock asymmetry	50 +/-5%, maximum
Differential voltage level (clock or data)	(A) to (B), 2 volts, minimum (see figure 1 - 8)
Time skew (clock or data)	(A) to (B) 6.5 nanoseconds, maximum
Time skew (data to clock)	(A) to (A) and (B) to (B), 25 % of a bit period, maximum
20% to 80% differential transition (rise and fall) time (data and clock)	12 nanoseconds, maximum
Output impedance	Less than 10 ohms
Panel connectors	Rear panel: 1A1J108, 15 pin female D type
PTE LOW DATA RATE BASEBAND DATA OUTPUTS	
Data format	NRZ or biphase
Data rate	1 kbps to 6 Mbps for NRZ, 1 kbps to 3 Mbps for biphase

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
PTE LOW DATA RATE BASEBAND DATA OUTPUTS (Continued)	
Clock rate	Same as data rate and synchronous with data for NRZ; twice the data rate and synchronous with data for biphase
Signal level	RS-422A
Signal type	Complementary balanced differential TTL
Clock asymmetry	50 +/-5%, maximum
Differential voltage level (clock or data)	(A) to (B), 2 volts, minimum (see figure 1 - 8)
Time skew (clock or data)	(A) to (B) 6.5 nanoseconds, maximum
Time skew (data to clock)	(A) to (A) and (B) to (B), 25 % of a bit period, maximum
20% to 80% differential transition (rise and fall) time (data and clock)	12 nanoseconds, maximum
Output impedance	Less than 10 ohms
Panel connectors	Rear panel: 1A1J110, 25 pin female D type
RECOVERED FORWARD DATA AND CLOCK OUTPUTS	
Data format	NRZ
Data rate	100 bps to 25 Mbps
Clock rate	Same as data rate and synchronous with data
Signal level (clock or data)	Differential (A) to (B) voltage, 400 mV, minimum
Signal type	Complementary balanced differential TTL
Nominal source impedance	Less than 10 ohms
Clock asymmetry	50 +/-5%, maximum

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
RECOVERED FORWARD DATA AND CLOCK OUTPUTS (Continued)	
Time skew (data to clock)	(A) to (A) and (B) to (B), 6.5 nanoseconds, maximum
20% to 80% differential transition (rise and fall) time (data and clock)	18 nanoseconds, maximum
Output impedance	Less than 10 ohms
Panel connectors	Rear panel: 1A1J111, 37 pin female D type
TRANSMIT CLOCK OUTPUTS	
Clock rate	100 Hz to 25 MHz for command channel BERTS; 100 Hz to 12 MHz for I and Q channel BERTS
Signal level	TTL
Signal type	Unbalanced single-ended TTL
Panel connectors	Rear panel: 1A1J104, 1A1J105, and 1A1J106, BNC female
DATA INPUTS	
Data rate	100 bps to 25 Mbps for command channel BERTS; 100 bps to 12 Mbps for I and Q channel BERTS
Signal level	TTL
Signal type	Unbalanced single-ended TTL
Data format	NRZ
Panel connectors	Rear panel: 1A1J115, 1A1J116, and 1A1J117, BNC female
RECOVERED DATA AND CLOCK OUTPUTS	
Data and clock rate	100 bps to 25 Mbps for command channel BERTS; 100 bps to 12 Mbps for I and Q channel BERTS. Clock rate is identical to and synchronous with the data rate

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
RECOVERED DATA AND CLOCK OUTPUTS (Continued)	
Signal level	TTL
Signal type	Unbalanced single-ended TTL
Data format	NRZ
Panel connectors	Rear panel: 1A1J120, 1A1J121, and 1A1J122, 1A1J123, 1A1J124, and 1A1J125 BNC female
70-MHz OUTPUT IF	
Nominal Frequency	70 MHz
Level	-55 dBm to +10 dBm
Panel connectors	Rear panel: 1A1J103, BNC female
70-MHz INPUT IF	
Nominal Frequency	70 MHz Level -55 dBm to +10 dBm (signal plus noise)
Panel connectors	Rear panel: 1A1J102, BNC female
370-MHz MODULATED OUTPUT IF	
Nominal Frequency	370 MHz
Level	0 dBm +/-3 dBm in a 30 MHz bandwidth
Stability of output power	+/-1 dB over any 1 hour period
Spurious signals	
Total RSS of all spurious signals	-30 dBc, maximum
Individual spurious signals (in or out of band)	-40 dBc, maximum
Nominal output impedance	50 ohms

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
370-MHz MODULATED OUTPUT IF (Continued)	
Output VSWR	1.3:1, maximum measured over a 19 MHz bandwidth centered at 370 MHz
Panel connectors	Rear panel: 1A1J119, SMA female
8.5-MHz IF OUTPUT	
Nominal Frequency	8.5 MHz
Level	0 dBm +/-3 dBm in a 15 MHz low pass bandwidth
Stability of output power	+/-1 dB over any 1 hour period
Spurious signals	
Total RSS of all spurious signals	-30 dBc, maximum
Individual spurious signals (in or out of band)	-40 dBc, maximum
Nominal output impedance	50 ohms
Output VSWR	1.3:1, maximum measured between 1 MHz and 10 MHz
Panel connectors	Rear panel: 1A1J118, SMA female
ACQUISITION PROCESSOR PWA	
Power Consumption	17.5 watts, typical; 23.6 watts, maximum
Input Power	+5.00 +/-0.25 Vdc; 3.5 amperes, typical; 4.5 amperes, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
DEMOD SYMBOL SYNCHRONIZER PWA	
Power Consumption	30 watts, maximum
Input Power	+5.00 +/-0.25 Vdc; 5.5 amperes, maximum -5.2 +/-0.25 Vdc; 0.2 ampere, maximum +12.0 +/-0.25 Vdc; 0.1 ampere, maximum -12.0 +/-0.25 Vdc; 0.1 ampere, maximum +15.0 +/-0.25 Vdc; 0.1 ampere, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Differential Inputs	TTL: 0.7 Vdc, minimum ECL: 0.7 Vdc, minimum
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
Differential Outputs	TTL: 2.0 Vdc, minimum ECL: 0.8 Vdc, minimum
TEST MODULATOR PWA	
Power Consumption	23.5 watts, maximum
Input Power	+5.00 +/-0.25 Vdc; 0.3 amperes, maximum -5.2 +/-0.25 Vdc; 0.3 ampere, maximum +15.0 +/-0.5 Vdc; 1.0 ampere, maximum -15.0 +/-0.5 Vdc; 0.35 ampere, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Differential Inputs	TTL: 0.7 Vdc, minimum ECL: 0.7 Vdc, minimum
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
Differential Outputs	TTL: 2.0 Vdc, minimum ECL: 0.8 Vdc, minimum

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
RF DOWN CONVERTER NO. 2	
Power Consumption	20 watts, maximum
Input Power	+5.00 +/-0.25 Vdc; 0.8 ampere, maximum -5.2 +/-0.25 Vdc; 0.4 ampere, maximum +15.0 +/-0.5 Vdc; 0.7 ampere, maximum -15.0 +/-0.5 Vdc; 0.2 ampere, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Differential Inputs	TTL: 0.7 Vdc, minimum ECL: 0.7 Vdc, minimum
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
Differential Outputs	TTL: 2.0 Vdc, minimum ECL: 0.8 Vdc, minimum
TIMING GENERATOR PWA	
Power Consumption	43 watts, maximum; 33 watts, typical
Input Power	+5.00 +/-0.25 Vdc; 5.4 amperes, maximum; 5.0 amperes, typical -5.2 +/-0.25 Vdc; 1.5 amperes, maximum; 0.75 amperes, typical +12.0 +/-1.2 Vdc; 1 milliampere, maximum; 1 microampere, typical -12.0 +/-1.2 Vdc; 1 milliampere, maximum; 1 microampere, typical +15.0 +/-1.5 Vdc; 0.2 amperes, maximum; 0.1 amperes, typical -15.0 +/-1.5 Vdc; 0.2 amperes, maximum; 0.1 amperes, typical
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc ECL Logic 0: -1.5 to -1.9 Vdc ECL Logic 1: -0.6 to -1.3 Vdc

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
TIMING GENERATOR PWA (Continued)	
Differential Inputs	TTL: 0.7 Vdc, minimum ECL: 0.7 Vdc, minimum 1553: 20 volts p-p, maximum
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc ECL Logic 0: -1.5 to -1.9 Vdc ECL Logic 1: -0.6 to -1.3 Vdc
Differential Outputs	TTL: 2.0 Vdc, minimum ECL: 0.8 Vdc, minimum 1553: per MIL-STD-1553
RF Outputs	Frequencies of 8.5 +/-0.25 MHz and 20 +/-1.6 MHz with a 50 ohm nominal impedance and at +/-2 dBm
SYNTHESIZER PWA	
Power Consumption	37 watts, maximum
Input Power	+5.00 +/-0.25 Vdc; 0.75 amperes, maximum -5.2 +/-0.25 Vdc; 0.75 amperes, maximum +15.0 +/-0.5 Vdc; 1.75 amperes, maximum -15.0 +/-0.5 Vdc; 0.2 amperes, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc ECL Logic 0: -1.85 to -1.63 Vdc ECL Logic 1: -0.98 to - 0.81 Vdc
PN PROCESSOR PWA	
Power Consumption	24.2 watts, maximum; 17.8 watts, typical
Input Power	+5.00 +/-0.25 Vdc; 4.0 amperes, maximum; 3.0 amperes, typical

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
PN PROCESSOR PWA (Continued)	
Input Power (Continued)	-5.2 +/-0.25 Vdc; 0.7 amperes, maximum; 0.48 amperes, typical +12.0 +/-0.25 Vdc; 19 milliamperes, maximum; 8 milliamperes, typical -12.0 +/-0.25 Vdc; 25 milliamperes, maximum; 16 milliamperes, typical
Logic Inputs	TTL Logic 0: 0.0 to 0.8 VdcT TTL Logic 1: 2.0 to 5.0 Vdc
Differential Inputs	ECL: 1 Vdc, minimum
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
DEMOD PROCESSOR PWA	
Power Consumption	21.0 watts, maximum; 15.0 watts, typical
Input Power	+5.00 +/-0.25 Vdc; 4.0 amperes, maximum; 3.0 amperes, typical +15.0 +/-1.5 Vdc; 30 milliamperes, maximum; 20 milliamperes, typical
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Logic Outputs	TTL Logic 0: 0.0 to 0.6 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
MODEM CONTROL PROCESSOR PWA	
Power Consumption	34 watts, maximum
Input Power	+5.00 +/-0.25 Vdc; 5.7 amperes, maximum +12.0 +/-0.25 Vdc; 0.2 ampere, maximum -12.0 +/-0.25 Vdc; 0.2 ampere, maximum

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
MODEM CONTROL PROCESSOR PWA (Continued)	
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
488 INTERFACE CONTROL PWA	
Power Consumption	20 watts, maximum
Input Power	+5.00 +/-0.25 Vdc; 2.0 amperes, maximum; 1.6 amperes, typical
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Logic Outputs	TTL Logic 0: 0.0 to 0.6 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
EXTERNAL CLOCK SYNCHRONIZER PWA	
Power Consumption	30.9 watts, maximum; 22.0 watts, typical
Input Power	+5.00 +/-0.25 Vdc; 4.0 amperes, maximum; 3.0 amperes, typical -5.2 +/-0.25 Vdc; 2.0 amperes, maximum; 1.3 amperes, typical
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc ECL Logic 0: -1.105 to -0.810 Vdc ECL Logic 1: -1.950 to -1.475 Vdc
Differential Inputs	ECL: 1 Vdc, minimum
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
TEST DATA INTERFACE PWA	
Power Consumption	32.0 watts, maximum
Input Power	+5.00 +/-0.25 Vdc; 2.5 amperes, maximum; 2.0 amperes, typical -5.00 +/-0.25 Vdc; 0.75 amperes, maximum TBD amperes, typical +15.0 +/-0.5 Vdc; 1.75 amperes, maximum +12.0 +/-0.5 Vdc; 0.2 amperes, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Differential Inputs	TTL: 0.7 Vdc, minimum ECL: 0.7 Vdc, minimum
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
Differential Outputs	TTL: 2.0 Vdc, minimum ECL: 0.8 Vdc, minimum
POWER SUPPLY NO. 2	
AC Input	90-132 Vac at 47-63 Hz
Efficiency	65% to 75%
Inrush Limiting	65 amperes maximum peak with electronic soft-start (150 amperes on 220 watts)
EMI Suppression	FCC Docket 20780, Class A and VDE 0871, Class A
Output Voltage	-5.2 +/-0.25 Vdc, adjustable; 30.0 amperes, maximum; 25 amperes, typical +12.00 +/-0.25 Vdc, adjustable; 5.0 amperes, maximum; 4.0 amperes, typical -12.00 +/-0.25 Vdc, adjustable; 6.0 amperes, maximum; 3.0 amperes, typical

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
POWER SUPPLY NO. 1	
AC Input	95-132 Vac at 47-440 Hz; Input power at maximum output power 633 watts
Efficiency	75% minimum at maximum output power
Inrush Limiting	75 amperes maximum
EMI Suppression	FCC Docket 20780, Class A and VDE 0871, Class A
Output Voltage	+5.00 +/-0.25 Vdc, adjustable; 75, 66, and 57 amperes maximum at 72, 90, and 108 degrees Fahrenheit, respectively; Minimum preload of 19.0 amperes is required on +5 Vdc output for maximum current on auxiliary outputs +15.00 Vdc +/-0.5 Vdc, adjustable; 7.2, 6.4, and 5.5 amperes maximum at 72, 90, and 108 degrees Fahrenheit, respectively -15.00 Vdc +/-0.5 Vdc, adjustable; 7.2, 6.4, and 5.5 amperes maximum at 72, 90, and 108 degrees Fahrenheit, respectively +5.00 (RF) Vdc +/-0.5 Vdc, adjustable; 7.2, 6.4, and 5.5 amperes maximum at 72, 90, and 108 degrees Fahrenheit, respectively
Output Power	475, 420, and 362 watts maximum at 72, 90, and 108 degrees Fahrenheit, respectively
POWER SUPPLY NO. 3	
AC Input	104-126 Vac at 50-60 Hz; 0.75 amperes at 115 Vac, maximum
Output Voltage	+130 Vdc at 0.18 amperes, maximum
Output Regulation	2%

Table 1 - 3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
TOUCH PANEL DISPLAY	
Panel Supply Voltage	+150 Vdc, maximum; +120 to +130 Vdc, nominal
Panel Current	160 milliamperes, +/-25%
Positive Logic Supply Voltage	+7.0 Vdc, maximum; 4.75 to 5.25 Vdc, nominal
Logic Current	2.0 amperes, +/-25%
High Level Logic (Data)	+7.0 Vdc, maximum; 2.4 to 5.5, nominal
Low Level Logic (Data)	-1.5 Vdc, maximum; -0.5 to 0.8 Vdc, nominal
High Level RS-232-C	+15.0 Vdc, maximum; 3 to 15 Vdc, nominal
Low Level RS-232-C	-15.0 Vdc, maximum; -3 to -15 Vdc, nominal

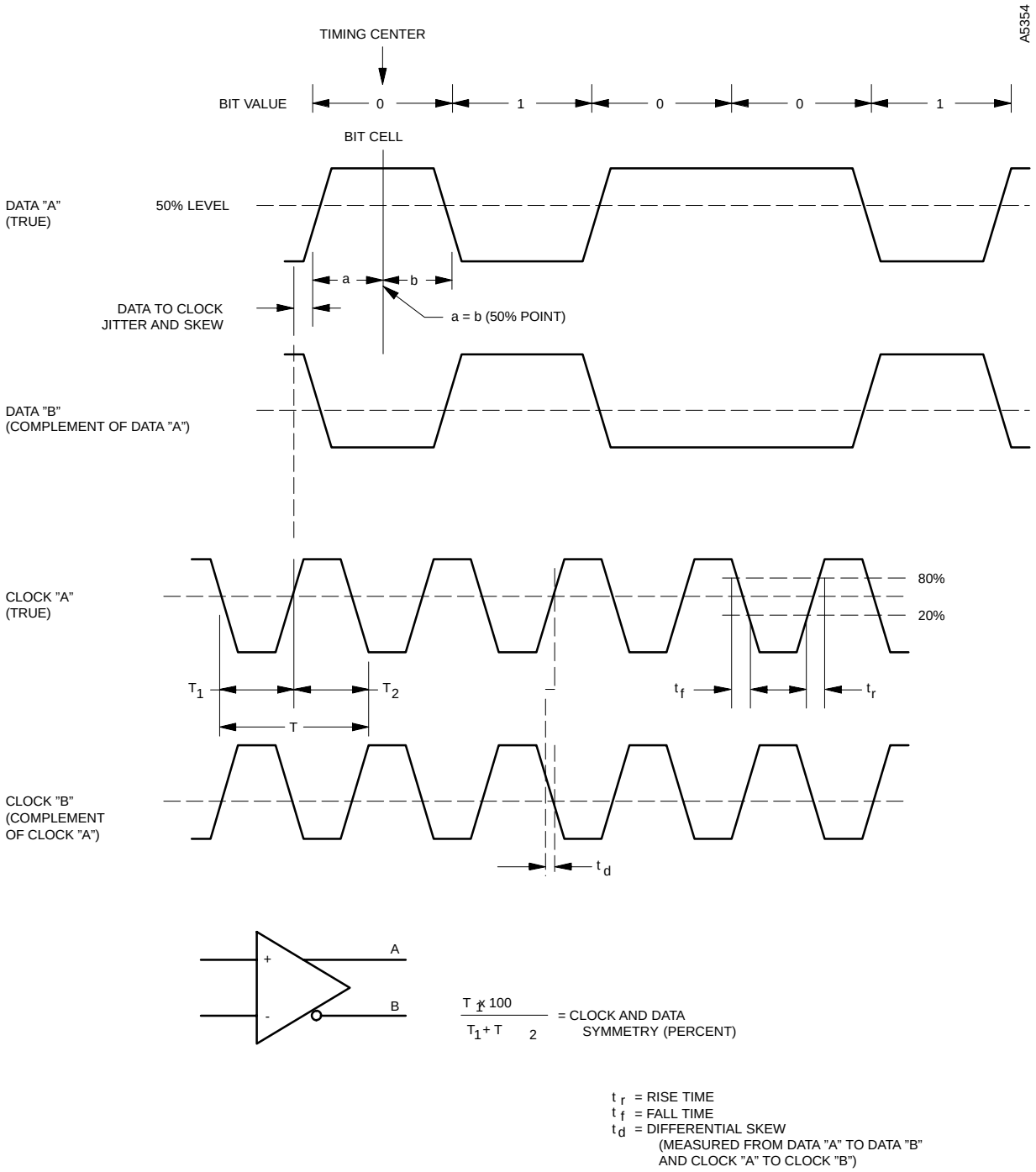


Figure 1 - 8. Differential Clock and Data Relationships

Table 1 - 4. NASA Drawings		
DRAWING NO.	DESCRIPTION	PAGE
Not applicable.		

Table 1 - 5. Environmental Requirements	
PARAMETER	DESCRIPTION
OPERATING ENVIRONMENT	
Temperature	+50 to +100 degrees Fahrenheit
Temperature rate	Temperature rate of change shall not exceed 10 degrees per hour
Humidity	From 20 to 80 percent without condensation
Altitude	Sea level to 12,000 feet
NONOPERATING ENVIRONMENT	
Temperature	-20 to +160 degrees Fahrenheit
Humidity	From 0 to 100 percent relative humidity, noncondensing environment
Altitude	Sea level to 35,000 feet
Solar Radiation	350 BTU/ft^2/hour

Table 1 - 6. Equipment Required, But Not Supplied		
MFR. MODEL/PART NO.	DESCRIPTION	PAGE
Not applicable.		

Table 1 - 7. Consumables			
NOMENCLATURE	SPECIFICATION NUMBER/NSN	PART NO./CAGE	APPLICATION
Not applicable.			

Table 1 - 8. Special Tools and Test Equipment				
RECOMMENDED MODEL/PART NO.	MANUFACTURER (FSCM)	COMMON NAME	USE	FIG. NO.
5120-00-278-1267	81348	No. 1 flat-tipped screw-driver	Remove/replace LRUs	N/A
5120-01 - 022-9953	55719	No. 1 cross-tipped screw-driver	Remove/replace LRUs	N/A
6625-01 - 235-2911	89356	Multimeter	Measure voltages/ resistances	N/A
6966-C	78976	Gun, heat	Heat shrink-wrap	N/A
Commercial source		Vacuum cleaner	Clean unit interior	N/A
Commercial source		Snub-nosed pliers	Remove/replace lampholder, switch	N/A
Commercial source		IC chip puller	Remove/replace MCP and DMDP IC chips	N/A
499-920-012	07421	Wirecutters/strippers	Remove/replace lampholder	N/A
499-925-014	07421	Soldering iron	Remove/replace	N/A

Section 2 — Installation

2–1 Introduction

This section contains chassis unpacking, installation, removal, packaging, and storage/shipment information for the Test Modem in the STGT. This section also includes a detailed view of the rear panel and associated connectors, figure 2-1. Refer to table 4-1 for connector pin identification information.

2–2 Chassis Installation in STGT

The TM is a complete unit and requires no internal wiring, strapping, or cable changes other than factory setup. The unit is designed to be housed in the USS KSA low data rate equipment HWCI cabinet, SSA equipment HWCI cabinet, or MA receiver/transmit equipment HWCI cabinet; the rack numbers are: 1006, 1012, 1015, 1024, 1029, 1013, and 1104. All external cable and wiring interfacing is site supplied.

2–3 Unpacking

The TM is shipped as a complete unit with all subassemblies (PWAs, power supplies, etc.,) installed. The unit is wrapped in antistatic bubble-wrap material and placed in a shipping container as shown in figure 2-2. To unpack the unit, proceed as follows:

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

NOTE

Before unpacking the unit, inspect the shipping container for signs of external damage. If the container is damaged, notify the carrier as well as the authorized field service personnel.

Keep the shipping container for future use, storage, or shipment for service/repair. Refer to the repackaging for shipment and storage paragraphs later in this section.

a. With the shipping container on the floor, topside up, open the shipping container by carefully cutting the plastic packing tape.

b. Remove the polyethylene packing material to gain access to the unit.

c. Remove the unit wrapped in antistatic bubble-wrap material. Remove the bubble-wrap from around the unit and place unit on floor (or other acceptable work area surface), topside up.

d. Perform a general inspection inventory of the major components (see table 1-2) to ensure the unit is complete.

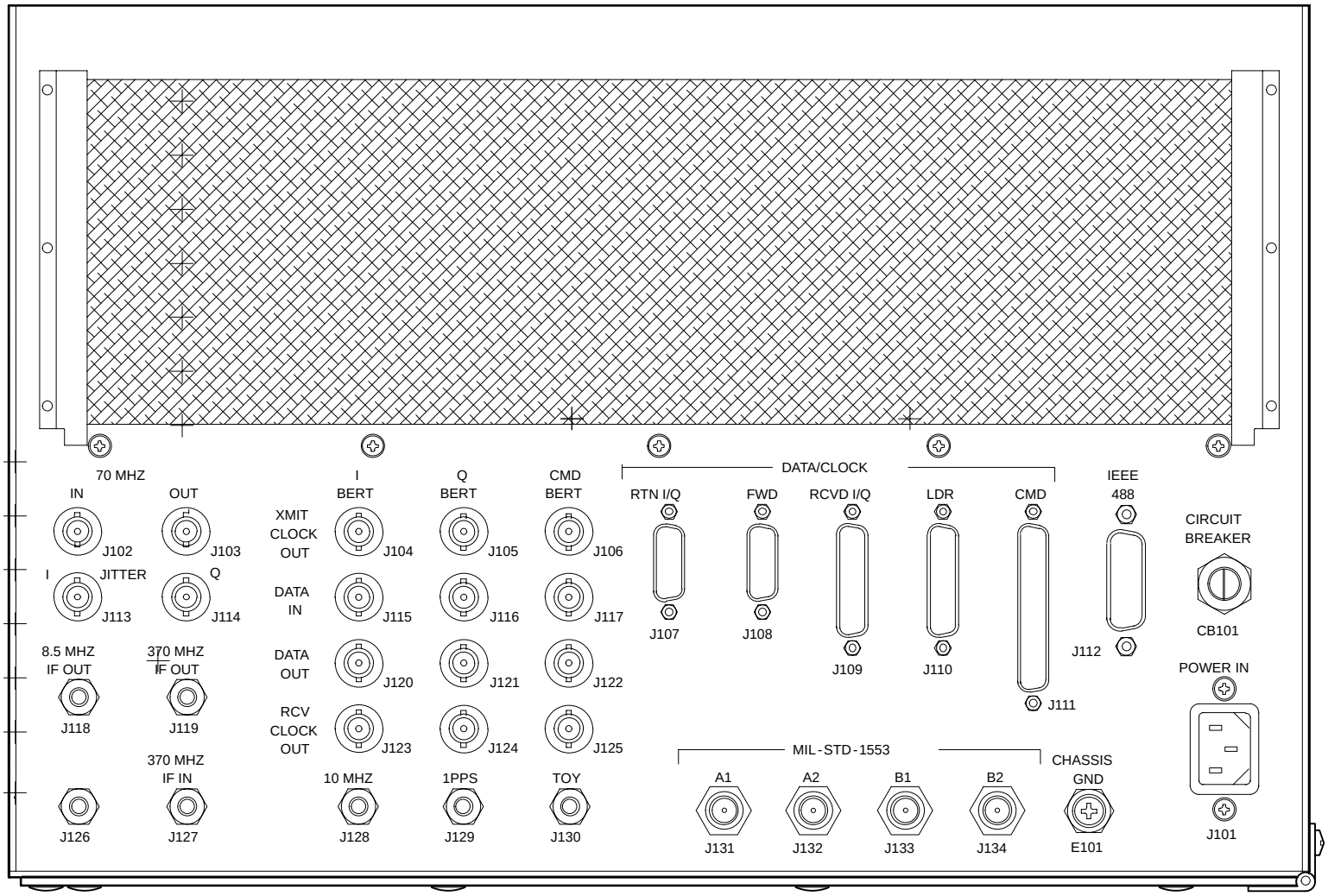
2–4 Chassis Installation

WARNING

The TM requires three people to safely lift and place/remove the unit into/from the cabinet assembly. Also, removing or installing items of equipment while the equipment cabinet is energized could result in damage to equipment or injury to personnel. Ensure that all power is removed from the equipment rack before attempting assembly.

The following procedure applies to all configurational uses of the TM.

a. Remove all electrical power from the equipment cabinet where the unit is to be installed.

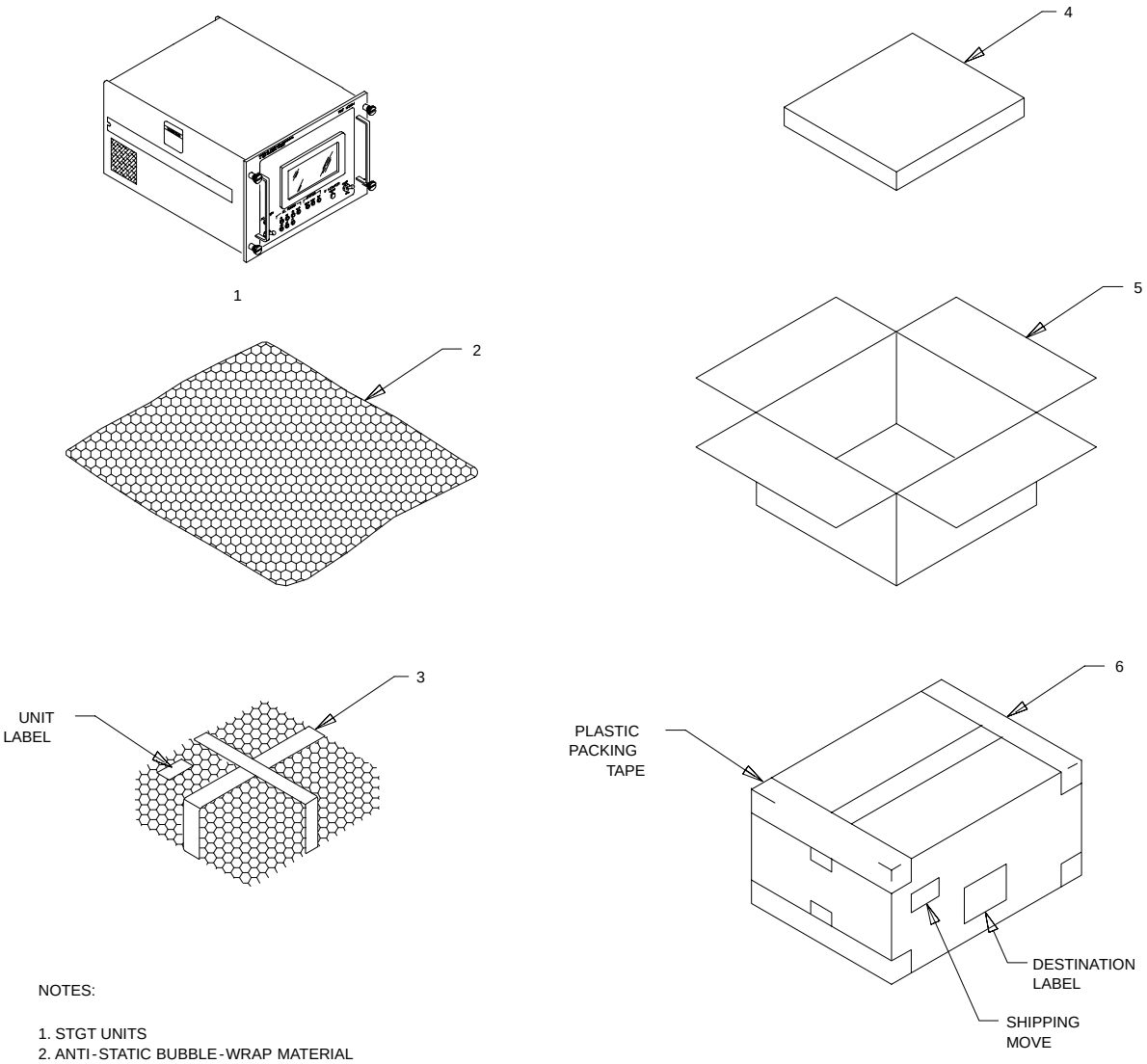


REAR VIEW

Figure 2 - 1. Test Modem Rear Panel

A4375

A5359



NOTES:

1. STGT UNITS
2. ANTI-STATIC BUBBLE-WRAP MATERIAL
3. WRAPPED UNIT(S)
4. ANTI-STATIC POLYETHYLENE PACKING MATERIAL
5. SHIPPING CONTAINER
6. SEALED SHIPPING CONTAINER

Figure 2 - 2. Equipment Packing/Unpacking

b. Gain access to the rear of the equipment cabinet assembly and ensure all cabling is clear for installation of unit.

c. Extend cabinet section rail guides until guide lock seats.

d. Raise the unit (three people required), with each person placing one hand on front panel handle and the other hand placed underneath the unit; guide the unit section slide rails into their respective cabinet rail guides until the quick lock/disconnect mechanism locks into position.

e. Disengage the rail guide locks and slide unit slowly into equipment cabinet to ensure a clear entry.

f. At rear of cabinet, attach all applicable cable connectors (use finger force on all SMA connectors) and grounding straps to unit. Refer to figures 1-3 or 1-4 and applicable site cable interfacing documentation, depending upon applicable configuration.

g. At the front of the unit, use a flat-tipped (common) screwdriver to tighten the four front-panel captive screws to the cabinet assembly.

h. Make a visual inspection to ensure that no cables are being pinched and that the unit is properly seated within the cabinet assembly.

i. Apply power to the cabinet assembly and all cabinet assembly units.

j. Perform the turn-on and self-check procedures found in section 3 to verify proper unit operation.

2–5 Chassis Removal

WARNING

The TM requires three people to safely lift and place/remove the unit into/from the cabinet assembly. Also, removing or installing items of equipment while the equipment cabinet is energized could result in damage to equipment or injury to personnel. Ensure that all power is removed from the equipment rack before attempting disassembly.

The following procedure describes the steps necessary to remove the TM from the equipment cabinet. Proceed as follows:

a. Perform the shutdown procedure found in section 3.

b. Remove all electrical power from the equipment cabinet.

c. Loosen the four captive screws holding the unit in the cabinet.

d. Gain access to the rear of the equipment cabinet assembly. Ensure that cables are properly tagged. Disconnect all cables and ground straps attached to the unit. Connect the 10-MHz cable to a 50 ohm dummy load.

e. Slide the unit forward until the rail guide locks are set to the locked position.

f. On each side of the unit, press the rail guide quick lock/disconnect mechanism and pull the unit forward just past the point where the mechanism locks. With three people, one on each side and one in front of the unit, each person placing one hand on front panel handle and the other hand underneath the unit, slide the unit out of the cabinet rail guides and place the unit on a workbench.

g. At the equipment cabinet, disengage the rail guide locks and slide the rail guides back into the cabinet.

2–6 Unit Packaging

The following procedure provides the necessary instructions to package the TM for storage or shipment. Refer to figure 2-2.

a. Obtain a quantity of antistatic bubble-wrap material (Federal Specification PPP-C-795, class 2) sufficient to wrap the unit to a thickness of at least 3-1/2 inches. Material must be of 1/2-inch thickness, and multiple wrappings must add up to a minimum of 3-1/2 inches.

b. Wrap unit with bubble-wrap and secure with masking tape.

c. Fill out a unit container label per STDN No. 507, Network Logistics Manual which includes the following information:

   (1) National stock number or activity control number

   (2) Part number

   (3) Part name

   (4) Serial number

   (5) Manufacturer's name

   (6) Quantity

d. Secure the label to the wrapped unit.

e. Place the maintenance report (when applicable) in an envelope. Identify on the envelope that it contains the maintenance report and attach the envelope to the unit.

f. Place unit in a cushioned shipping/storage container. The shipping/storage container should be in accordance with customer logistics procedures.

g. Place sufficient antistatic polyethylene packing material (type I) around the unit to ensure no movement during shipment.

h. Seal the container with plastic packing tape or other suitably strong tape.

i. Fill out a shipping label per STDN No. 507, Network Logistics Manual.

j. Place the shipping label in the upper left corner of the shipping container side.

k. Fill out the destination address label and place it in the center of the shipping container side.

2–7 PWA Packaging

The following procedure provides the necessary instructions to package a PWA for storage or shipment.

a. Obtain a quantity of antistatic bubble-wrap material (Federal Specification PPP-C-795, class 2) sufficient to wrap the PWA to a thickness of at least 1 inch. Material must be of 1/2-inch thickness, and multiple wrappings must add up to a minimum of 1 inch.

b. Wrap PWA with bubble-wrap and secure with masking tape.

c. Fill out a PWA container label per STDN No. 507, Network Logistics Manual which includes the following information:

   (1) National stock number or activity control number

   (2) Part number

   (3) Part name

   (4) Serial number

   (5) Manufacturer's name

   (6) Quantity

d. Secure the label to the wrapped PWA.

e. Place the maintenance report (when applicable) in an envelope. Identify on the envelope that it contains the maintenance report and attach the envelope to the PWA.

f. Place PWA in a cushioned shipping/storage container. The shipping/storage container should be in accordance with customer logistics procedures.

g. Place sufficient antistatic polyethylene packing material (type I) around the PWA to ensure no movement during shipment.

h. Seal the container with plastic packing tape or other suitably strong tape.

i. Fill out a shipping label per STDN No. 507, Network Logistics Manual.

j. Place the shipping label in the upper left corner of the shipping container side.

k. Fill out the destination address label and place it in the center of the shipping container side.

2–8 Storage

2–8.1 Short–Term Storage

For short-term storage the unit suffers no permanent degradation or damage when stored under the following environmental conditions:

a. Temperature: -20 to 160 degrees Fahrenheit.

b. Humidity: 0 to 100 percent relative humidity, noncondensing environment.

c. Altitude: Sea level to 35,000 feet.

2–8.2 Long–Term Storage

For long-term storage repackage the unit up to step (g) of the packaging procedure in paragraph 2-6 or 2-7. The unit suffers no permanent degradation or damage when stored under the environmental conditions specified in paragraph 2-8.1.

2–9 Shipment

Package the unit/PWA for shipment according to the procedure in paragraph 2-6 or 2-7. Ship the packaged unit by best commercial method.

Section 3 — Operation

3–1 Introduction

This section contains information and procedures to aid personnel in operating and maintaining the Test Modem. A complete identification of all operating controls and indicators is included. Prior to performing maintenance, the paragraphs and procedures in this section must be understood and implemented.

WARNING

All personnel are required to read and understand paragraph 3 - 5, SAFETY, prior to performing any operations, removal/replacement, connections, and/or hardware tests on chassis. Failure to do so can cause death, injury, or equipment damage.

3–2 Modes of Operation

The TM has three operating modes: online, hot standby mode, and maintenance/software delivery (offline) mode. These modes are all remotely controlled. All three equipment modes are enabled when the front panel REMOTE/LOCAL switch is in the REMOTE position (remote control), and local control is enabled when the REMOTE/LOCAL switch is in the LOCAL position (local control). The TM must be offline in order to perform maintenance on the TM. The offline condition can be enabled by the TDRSS Operations Control Center No. 2 (TOCC2) operator when remote control is active or by placing the REMOTE/LOCAL switch to the LOCAL position.

3–3 Remote Control

The normal operating mode of the TM is remote control (front panel LOCAL/REMOTE switch placed in the remote position). Remote control of the TM is handled by the automated data processing equipment (ADPE) interfaced to the TM via the 1553 bus. Refer to STGT USS TOCC2 operators manual for normal/maintenance operations of the TM during remote control operation.

3–4 Local Control

Local control of the TM is strictly a maintenance mode. By placing the LOCAL/REMOTE switch in the local position, an operator is enabling the extended (offline) BIT function to be initiated from the front panel. By placing the TM in the local control condition, the unit cannot progress past the standby state (refer to section 4 for an explanation of the TM states of operation). To perform maintenance operations on the TM during local control, refer to section 5.

3–5 Safety

The following are warnings that are generally applicable when working near or inside equipment containing high voltage or other hazards that can cause death or injury and equipment damage. All warnings contained herein must be read and understood before proceeding with any removal/replacement, hardware tests, and/or connections on the TM. Throughout this manual, specific warnings, cautions, and notes appear immediately before each paragraph or procedural step to which they pertain.

WARNING

USE EXTREME CAUTION WHEN PERFORMING THE PROCEDURES IN THIS MANUAL. Contact with energized circuits can cause personal injury or death. Personnel should be familiar with CPR.

REMOVE RINGS, BRACELETS, WRISTWATCH, NECKCHAINS, AND OTHER METAL BEFORE WORKING AROUND

ELECTRONIC/MECHANICAL EQUIPMENT. Jewelry can get caught and cause injury, or can cause a short circuit on contact and cause severe burns and electrical shock.

WHEN AN ABNORMAL CONDITION EXISTS AND PERTINENT PROCEDURES DO NOT APPLY, STOP THE MAINTENANCE ACTIONS AND OBTAIN EXPERT GUIDANCE. Failure to comply could lead to death or injury and equipment damage.

3–6 Equipment Access

To perform local control operations of the TM, the unit must be extended to gain access to the maintenance panel. Loosen the four captive screws holding the unit in the cabinet. Slide the unit forward until the rail guide locks are set to the locked position.

3–7 Controls and Indicators

Before proceeding with any operation with the TM, refer to paragraph 3-5. Figures 3-1 through 3-4 illustrate the various controls and indicators of the TM. Tables 3-1 through 3-5 contain a complete list of the panel operating controls and indicators, including reference designators and brief functional descriptions.

3–8 Displays and Menus

Before proceeding with any operation with the TM, refer to paragraph 3-5. The TM utilizes an interactive touch panel display which combines an alpha-numeric gas discharge dot matrix display (12x40 characters) with touch-input infrared switches. Interaction is achieved by the operator reading the display and responding by finger or pointer contact to the touch-sensitive switch location on the viewing screen. Refer to figures 3-5 through 3-20 for the TM displays.

3–9 Display Menu Hierarchy

The TM displays hierarchy is as follows:

SELECT MENU (figure 3-5)

- MAINTENANCE MENU (figure 3 - 6)
  - EXTENDED BIT SUMMARY MENU (figure 3 - 7)
    - BIT RESULTS DISPLAY (tests 1 through 8; figure 3 - 8)
    - BIT RESULTS DISPLAY (tests 9 through 12; figure 3 - 9)
    - OFFLINE BIT DETAIL DISPLAY (test 1 through 8; figure 3 - 8A)
    - OFFLINE BIT DETAIL DISPLAY (tests 9 through 12; figure 3 - 9A)
    - LRU DEFINITION DISPLAY (figure 3 - 10)
  - CONFIDENCE TEST RESULTS DISPLAY (figure 3 - 11)
    - CONFIDENCE TEST DETAIL DISPLAY (figure 3 - 11A)
  - ONLINE BIT RESULTS DISPLAY (figure 3 - 12)
    - ONLINE BIT DETAIL DISPLAY (figure 3 - 12A)
  - FIRMWARE VERSION DISPLAY (figure 3 - 13)
    - CMD CHANNEL TEST POINT SELECTION MENU #1 (figure 3 - 14)
    - CMD CHANNEL TEST POINT SELECTION MENU #2 (figure 3 - 15)
  - CONFIGURATION MENU (figure 3 - 16)
    - RETURN MODULATOR SERVICE CONFIG DISPLAY (figure 3 - 17)
    - RETURN MODULATOR CONFIG DISPLAY (figure 3 - 18)
    - FORWARD DEMODULATOR SERVICE CONFIG DISPLAY (figure 3 - 19)
    - CONFIGURATION OVERRIDES DISPLAY (figure 3 - 21)
  - RETURN SERVICES DISPLAY (FWD DEMOD STATUS; figure 3 - 20)

Below is a list of explanations for display/operator interaction.

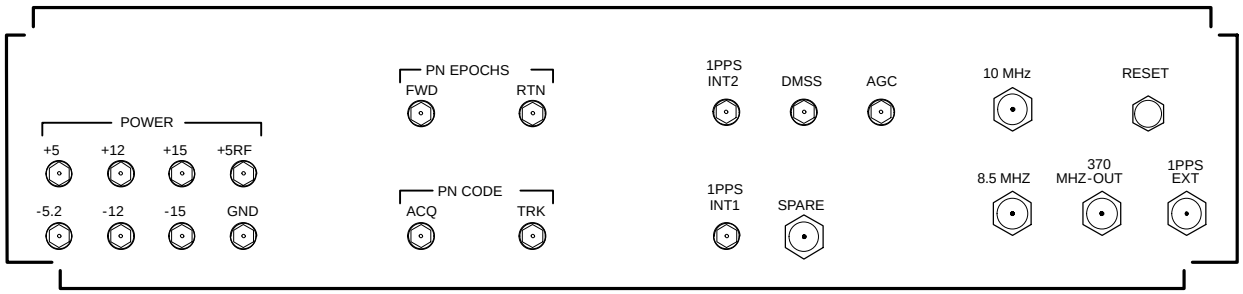
a. An invalid touch key selection produces an “INVALID SELECTION” message in the right upper hand top corner of display.

b. The bottom left corner of each display returns the display to the previous menu level. If the menu level is zero (highest), then touching the bottom left corner results in the display being refreshed.

c. The upper left corner of every display contains the current time of day.

d. The selected display is updated once every second.

A4385



A4384

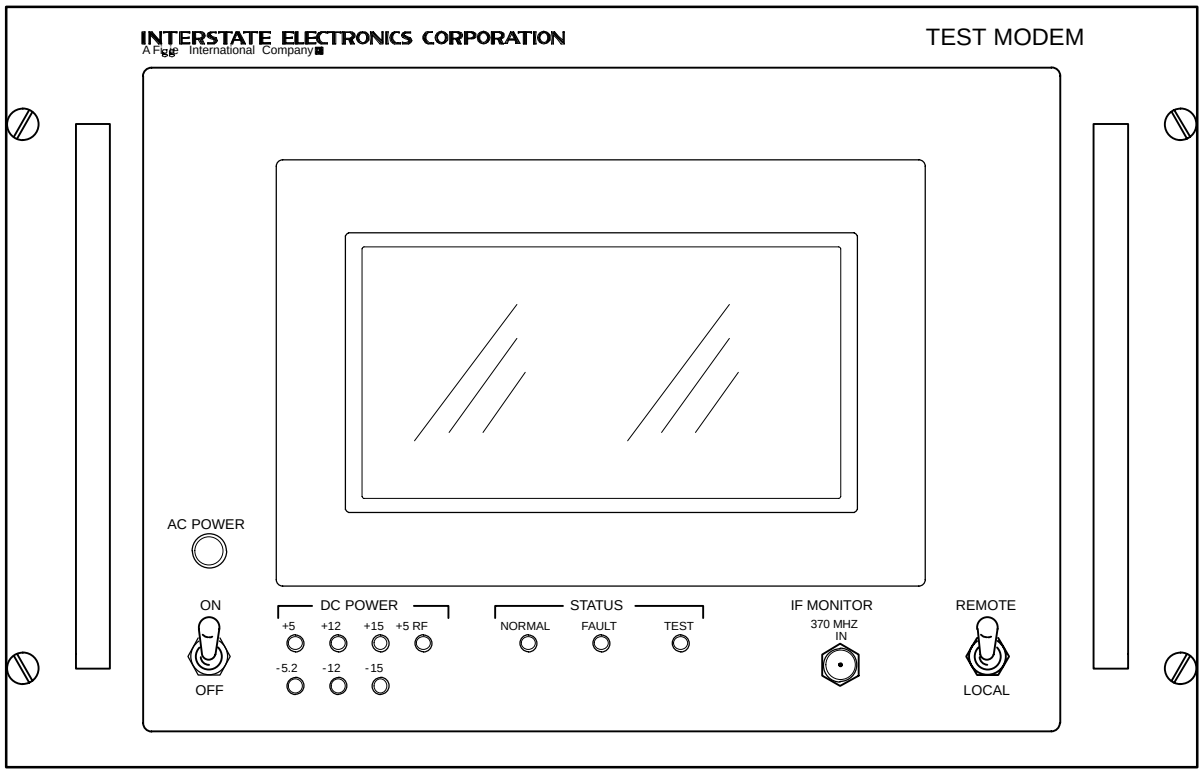
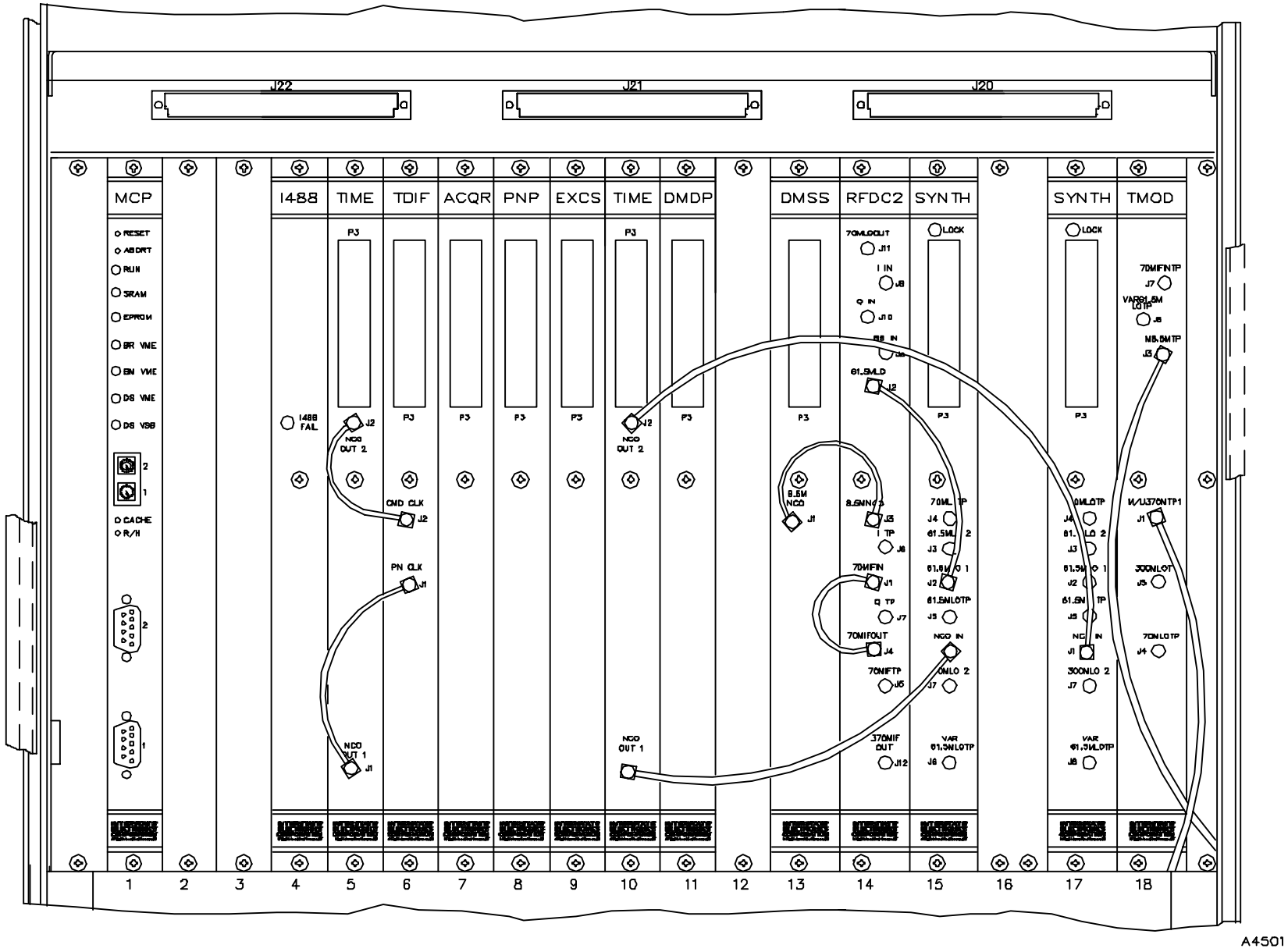
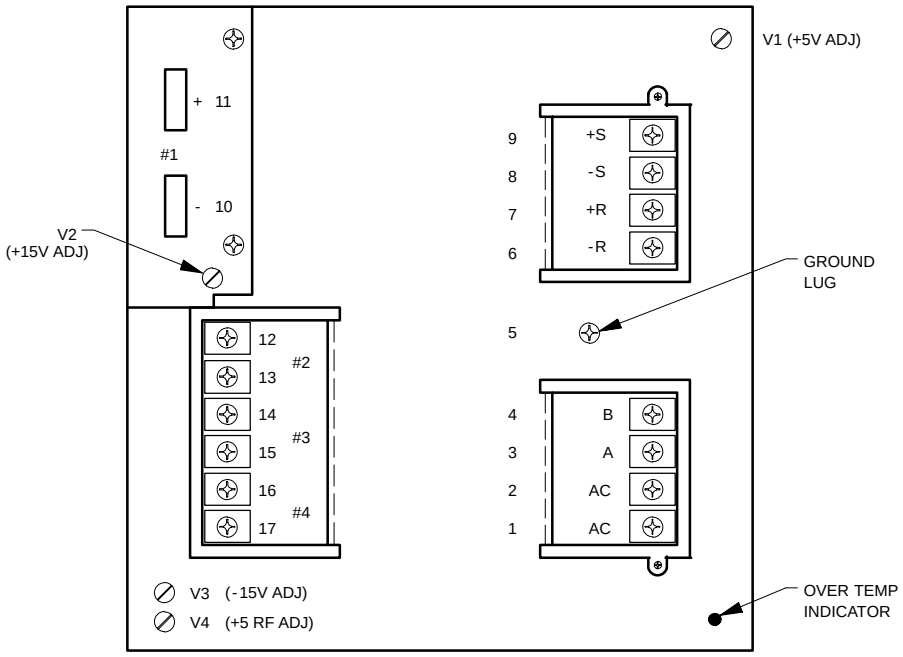


Figure 3 - 1. Front and Maintenance Panels



3 - 2. PWA Front Panels

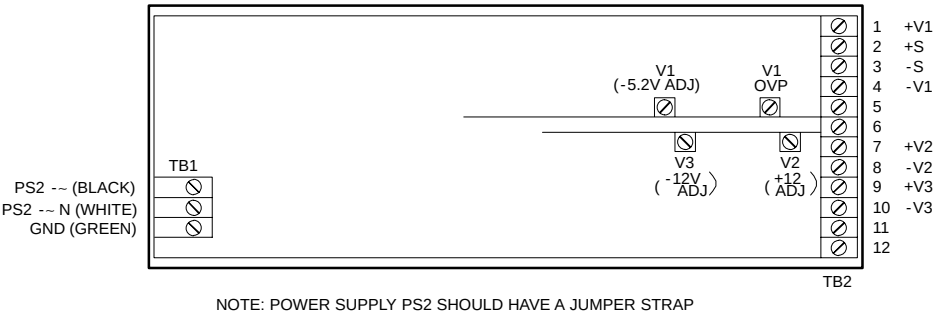
A5302



NOTE: POWER SUPPLY PS1 SHOULD HAVE A JUMPER STRAP FROM 3 TO 4.

Figure 3 - 3. Power Supply No. 1 Controls and Indicators

A5303



NOTE: POWER SUPPLY PS2 SHOULD HAVE A JUMPER STRAP FROM TB2-1 TO TB2-2, AND TB2-3 TO TB2-4.

Figure 3 - 4. Power Supply No. 2 Controls

Table 3 - 1. Front Panel Controls and Indicators

FIG REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3 - 1	“Display”	1A7A1	Touch panel display	Interactive touch panel and display
3 - 1	AC POWER	1A7DS1	Indicator	Turns on green to indicate ac power has been distributed through unit
3 - 1	ON/OFF	1A7SW1	Toggle switch	Primary power on/off control
3 - 1	DC POWER			
	+5	1A7DS2	Indicator	Turns on green to indicate +5 Vdc power supply is activated
	+12	1A7DS3	Indicator	Turns on green to indicate +12 Vdc power supply is activated
	+15	1A7DS4	Indicator	Turns on green to indicate +15 Vdc power supply is activated
	+5 RF	1A7DS5	Indicator	Turns on green to indicate RF +5 Vdc power supply is activated
	- 5.2	1A7DS9	Indicator	Turns on green to indicate - 5.2 Vdc power supply is activated
	- 12	1A7DS10	Indicator	Turns on green to indicate - 12 Vdc power supply is activated
	- 15	1A7DS11	Indicator	Turns on green to indicate - 15 Vdc power supply is activated
3 - 1	STATUS			
	NORMAL	1A7DS6	Indicator	Turns on green to indicate that the unit is in normal operation and has passed extended BIT or confidence BIT
	FAULT	1A7DS7	Indicator	Turns on red to indicate that the unit has detected a fault as a result of the confidence, extended, or online BIT
	TEST	1A7DS8	Indicator	Turns on amber to indicate that the unit is in process of performing extended BIT or confidence BIT

Table 3 - 1. Front Panel Controls and Indicators (Continued)

FIG REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3 - 1	IF MONITOR 370 MHZ IN	1A7J1	Test point	Tap - off of the 370 - MHz IF input to RFDC2
3 - 1	LOCAL/ REMOTE	1A7SW2	Toggle switch	LOCAL: Locks out the 1553 bus interface and allows the operator to command the extended BIT from the touch panel display REMOTE: Locks out any operator control from the touch panel display and enables unit control from the 1553 Bus

Table 3 - 2. Maintenance Panel Controls and Indicators

FIG REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3 - 1	POWER			
	+5	1A6TP1	Test point	PS No. 1 generated +5 Vdc signal
	+12	1A6TP2	Test point	PS No. 2 generated +12 Vdc signal
	+15	1A6TP3	Test point	PS No. 1 generated +15 Vdc signal
	- 5.2	1A6TP4	Test point	PS No. 2 generated - 5.2 Vdc signal
	- 12	1A6TP5	Test point	PS No. 2 generated - 12 Vdc signal
	- 15	1A6TP6	Test point	PS No. 1 generated - 15 Vdc signal
	+5 RF	1A6TP7	Test point	PS No. 1 generated RF +5 Vdc signal
	GND	1A6TP8	Test point	Power supply ground
3 - 1	PN EPOCHS FWD	1A6TP9	Test point	PNP generated signal (Tracking PN Epoch) used to identify start of forward service (demodulator mode) PN code signal (active low)

Table 3 - 2. Maintenance Panel Controls and Indicators (Continued)

FIG REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3 - 1	RTN	1A6TP10	Test point	TDIF generated signal used to identify start of return service (modulator mode) PN code signal (active low)
3 - 1	PN CODE			
	ACQ	1A6TP9	Test point	PNP generated quadrature phase acquisition PN code signal; Used by DMSS acquisition correlators during demodulator mode for forward service verification of MDP
	TRK	1A6TP10	Test point	PNP generated quadrature phase ontime tracking PN code signal; Used by DMSS for tracking and error detection during demodulator mode for forward service verification of MDP
3 - 1	1PPS INT1	1A6TP14	Test point	TIME1 generated 1 - Hz TTL signal with a 20% duty cycle and valid on the falling edge; Based upon the 50 - MHz signal input from the SYNTH1 PWA and the 1PPS external input
3 - 1	1PPS INT2	1A6TP15	Test point	TIME2 generated 1 - Hz TTL signal with a 20% duty cycle and valid on the falling edge; Based upon the 50 - MHz signal input from the TIME1 PWA
3 - 1	DMSS	1A6TP11	Test point	Analog representation of test points 0 - 7 located atop DMSS PWA (card slot 13); This signal is based upon test selection controlled by firmware
3 - 1	1PPS EXT	1A6J5	Connector	Connector access to 1PPS external input at J129
3 - 1	AGC	1A6TP16	Test point	DMDP generated analog gain control signal used to control the RFDC2 70 - MHz IF signal
3 - 1	10 MHZ	1A6J1	Connector	Connector access to 10 - Mhz reference frequency external input
3 - 1	RESET	1A6SW3	Pushbutton switch	Initiates initialization and self - test of unit during any operating state

Table 3 - 2. Maintenance Panel Controls and Indicators (Continued)

FIG REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3 - 1	8.5 MHZ	1A6J4	Connector	TMOD generated 8.5 - MHz subcarrier downconverted from the 70 - MHz IF signals plus noise returned from the noise test set; Downconverted by the 61.5 - MHz LO which allows Doppler simulation and supports MA, SSA, and KSA center frequency assignments
3 - 1	370 MHZ-OUT	1A6J2	Connector	TMOD generated modulated/ unmodulated 370 - MHz IF signal upconverted from the 70 - MHz IF signal plus noise input from the noise test set; The upconversion is accomplished by modulating it with a 300 - MHz LO from SYNTH2
3 - 1	SPARE	1A6J3	Connector	Not used

Table 3 - 3. PWA Controls and Indicators

FIG REF.	PWA NAME	PANEL MARKING	TYPE OF DEVICE	FUNCTION
3 - 2	Modem Control Processor PWA	RESET	Switch	A reset of all onboard I/O devices and the FPCP is enabled if the RESET switch is pushed to the “up” position. RESET is held active until the switch is in the “down” position; In addition, a local timer guarantees a minimum reset time of 2 to 3 seconds; Power fail and power up also force a reset (2 - 3 seconds) to start the board if the supply voltage is out of range (below 4.75 volts)
		ABORT	Switch	The ABORT switch, which provides an interrupt on a software - programmable level, is provided on the board to allow an abort of the current program, to trigger a self - test, or to start a maintenance program; ABORT is activated in the “up” position and deactivated in the “down” position

Table 3 - 3. PWA Controls and Indicators (Continued)

FIG REF.	PWA NAME	PANEL MARKING	TYPE OF DEVICE	FUNCTION
3 - 2	Modem Control Processor PWA (Continued)	RUN	Indicator	The RUN LED is green if the processor is not in the halt state; It is red during the reset phase or when the processor is in the halt state
		SRAM	Indicator	The SRAM LED is always lit yellow when the processor is accessing the local SRAM
		EPROM	Indicator	The EPROM LED is lit yellow when the processor accesses the EPROM area
		BR VME	Indicator	The bus request (BR) VME LED is lit yellow when the local processor requests bus mastership on the VMEbus
		BM VME	Indicator	The bus master (BM) LED is lit when the MCP is the current bus master
		DS VME	Indicator	The data strobe (DS) VME LED is lit whenever the processor has placed a data strobe on the VMEbus
		DS VSB	Indicator	The DS VSB LED is lit whenever the processor has placed a data strobe on the VSB
		1, 2	Switch	The rotary switches are 4 - bit hexadecimal encoded; They are completely under software control
		CACHE	Switch	The CACHE switch enables the 68030 onchip data cache with its 256 bytes when in the “down” position; In the “up” position, the onchip cache is deactivated by hardware, overriding all software settings
		R/H	Switch	The RUN/HALT (R/H) switch enables or disables local operation of the CPU and the FPCP; This switch can be used to debug multiprocessor software packages and to disable a CPU board in an application when a failure has occurred but power can’t be switched off; The processor is in the halt state if the switch is in the “up” position; Normal operation is provided when the switch is in the “down” position

Table 3 - 3. PWA Controls and Indicators (Continued)

FIG REF.	PWA NAME	PANEL MARKING	TYPE OF DEVICE	FUNCTION
3 - 2	Synthesizer PWA	LOCK	Indicator	Turns on to indicate that the 61.5 - MHz PLL, 140 - MHz PLL, and 10 - MHz reference input are normal
3 - 2	488 Interface Control PWA	I488 FAIL	Indicator	Turns on to indicate that IEEE - 488 interface to VMEbus interface has failed

Table 3 - 4. Power Supply No. 1 Controls and Indicators

FIG. REF.	FIGURE MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3 - 3	V1 (+5V ADJ)	1A2V1	Potentiometer	Used to adjust the +5.0 Vdc output voltage
3 - 3	V2 (+15V ADJ)	1A2V2	Potentiometer	Used to adjust the +15.0 Vdc output voltage
3 - 3	V3 (- 15V ADJ)	1A2V3	Potentiometer	Used to adjust the - 15.0 Vdc output voltage
3 - 3	V4 (+5RF ADJ)	1A2V4	Potentiometer	Used to adjust the +5.0 RF Vdc output voltage
3 - 3	OVER TEMP INDICATOR	1A2DS1	Indicator	Turns on to indicate a fan failure

Table 3 - 5. Power Supply No. 2 Controls

FIG. REF.	FIGURE MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3 - 4	V1 OVP	1A3V1A	Potentiometer	Used to adjust the overvoltage protection threshold voltage level for the - 5.2 Vdc output voltage
3 - 4	V1 (- 5.2V ADJ)	1A3V1B	Potentiometer	Used to adjust the - 5.2 Vdc output voltage
3 - 4	V2 (+12V ADJ)	1A3V2	Potentiometer	Used to adjust the +12.0 Vdc output voltage
3 - 4	V3 (- 12V ADJ)	1A3V3	Potentiometer	Used to adjust the - 12.0 Vdc output voltage

NOTE

The TM displays provide the following information:

1. eeeeeeeeeee = error messages.
2. hh = { 0 to 23}; mm = { 0 to 59}; ss = { 0 to 59}.

hh:mm:ss SELECT MENU eeeeeeeeeee

[ ] Maintenance
[ ] Configuration
[ ] TM Services

[ ] Display Refresh

Figure 3 - 5. Select Menu

hh:mm:ss MAINTENANCE eeeeeeeeeee

[ ] EXTENDED BIT
[ ] CONFIDENCE BIT
[ ] ONLINE BIT

[ ] DISPLAY FIRMWARE VERSION

[ ] SELECT CMD CHANNEL TO TEST POINT

[ ] PREVIOUS MENU

Figure 3 - 6. Maintenance Menu

hh:mm:ss EXTENDED BIT SUMMARY eeeeeeeeeee

		LRUs	Detail
TESTS 1 - 8	XXXXXXXX	[ ]	[ ]
TESTS 9 - 12	XXXX	[ ]	[ ]

[ ] START BIT [ ] HALT BIT

[ ] PREVIOUS MENU

NOTES:
1. X = {" "; P; F}, WHERE " " = TEST HAS NOT RUN YET; P = TEST PASSED; AND F = TEST FAILED (ONE OR MORE BAD PWAs).
2. THE "START BIT" SELECTION IS ENABLED ONLY WHEN THE UNIT IS IN LOCAL. IF SELECTED WHEN THE UNIT IS IN REMOTE, THE ERROR MESSAGE "NOT LOCAL" IS DISPLAYED.

Figure 3 - 7. Extended BIT Summary Menu

hh:mm:ss BIT RESULTS eeeeeeeeeee

MCP	X	00000	00000	00000	00000	00000
VME	X	00000	00000	00000	00000	00000
TIME	X	00000	00000	00000	00000	00000
DMDP	X	00000	00000	00000	00000	00000
ASICQ	X	00000	00000	00000	00000	00000
SGLVL	X	00000	00000	00000	00000	00000
PNP	X	00000	00000	00000	00000	00000
CORR	X	00000	00000	00000	00000	00000

[ ] SUMMARY [ ] LRU DEF. [ ] TESTS 9 - 12

NOTES:
1. X = {" "; P; F}, WHERE " " = TEST HAS NOT RUN YET; P = TEST PASSED; AND F = TEST FAILED (ONE OR MORE BAD PWAs).
2. 0 = { - ; G; S}, WHERE G = LRU GOOD; S= LRU SUSPECT; AND - = NOT APPLICABLE or TEST NOT RUN YET.
3. EACH TEST RESULT COLUMN CORRESPONDS TO AN LRU. SEE FIGURE 3-10 FOR LRU - COLUMN NUMBER CORRESPONDENCE.

Figure 3 - 8. BIT Results (Tests 1 - 8) Display

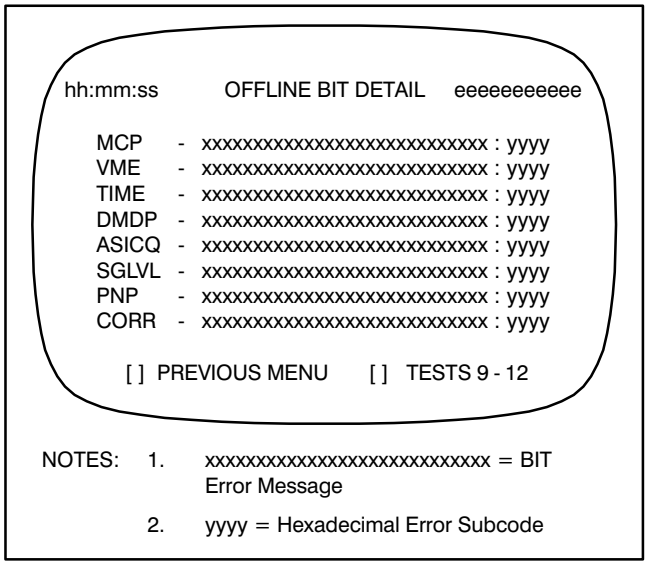


Figure 3 - 8A. Offline BIT Detail (Tests 1 - 8) Display

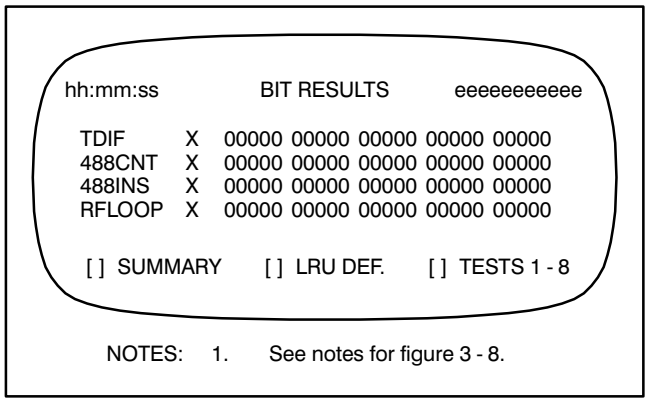


Figure 3 - 9. BIT Results (Tests 9 - 12) Display

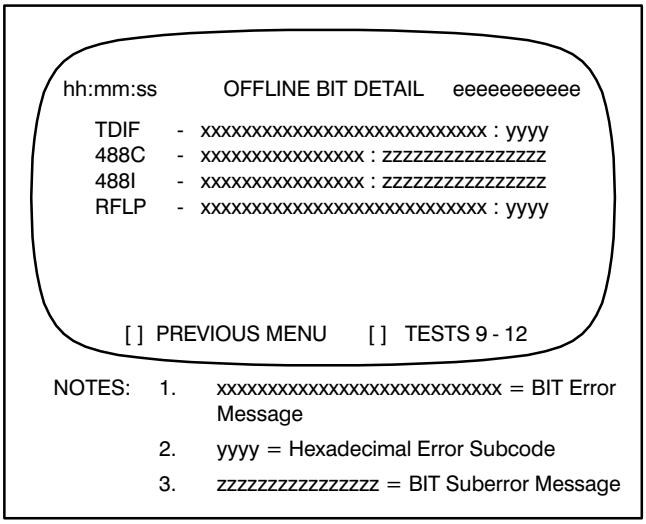


Figure 3 - 9A. Offline BIT Detail (Tests 9 - 12) Display

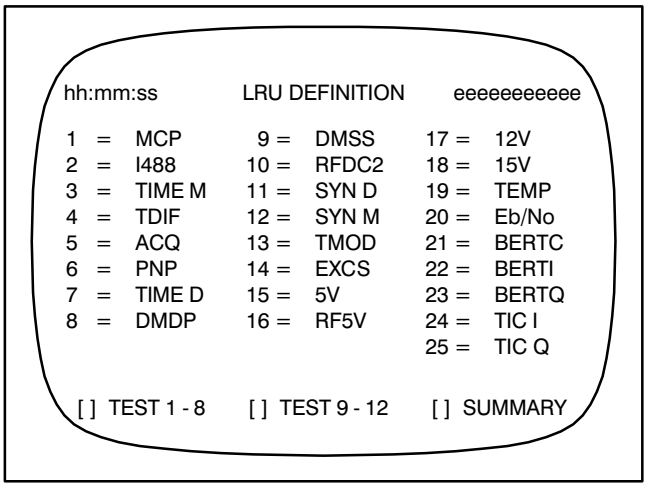


Figure 3 - 10. LRU Definition Display

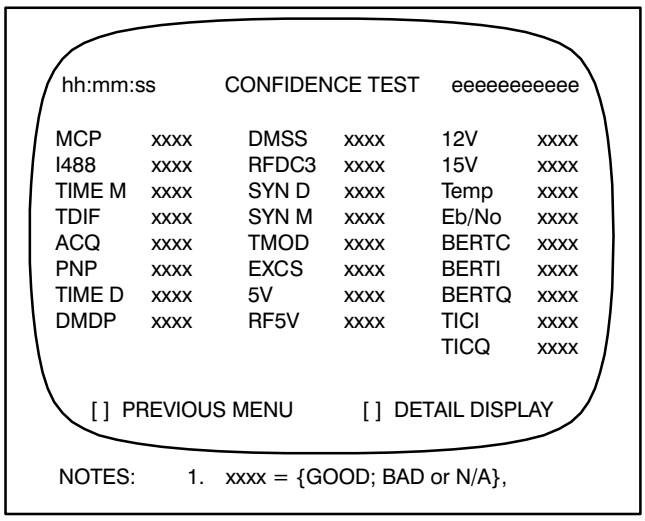


Figure 3 - 11. Confidence Test Results Display

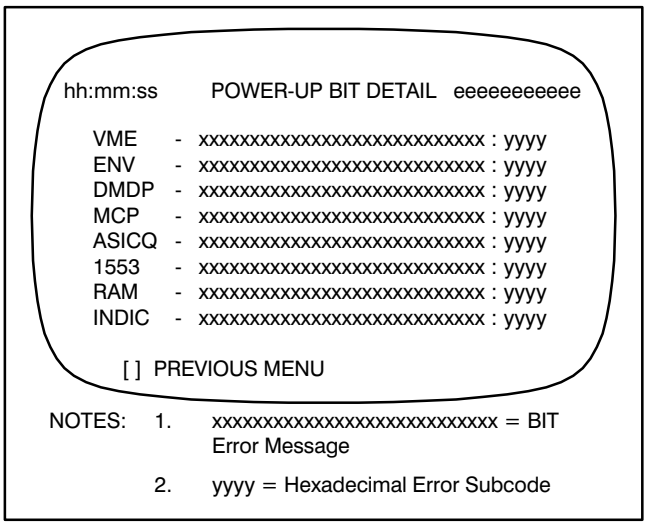


Figure 3 - 11A. Confidence Test Detail Display

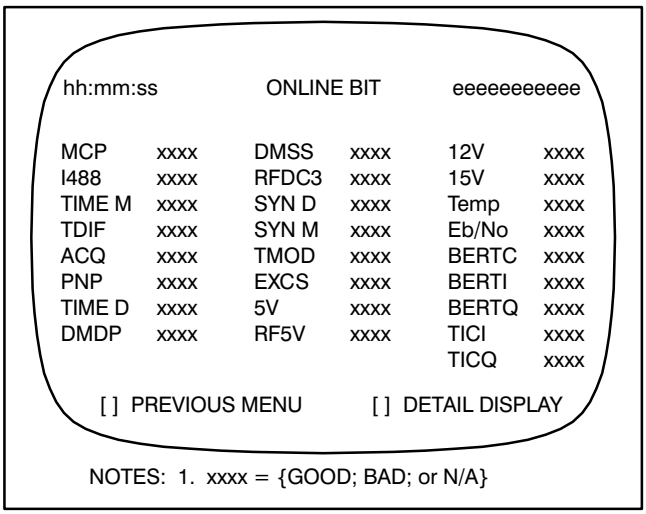


Figure 3 - 12. Online BIT Results Display

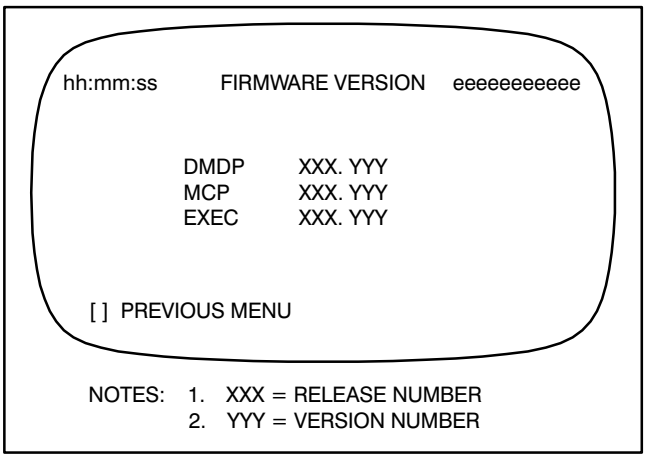


Figure 3 - 13. Firmware Version Display

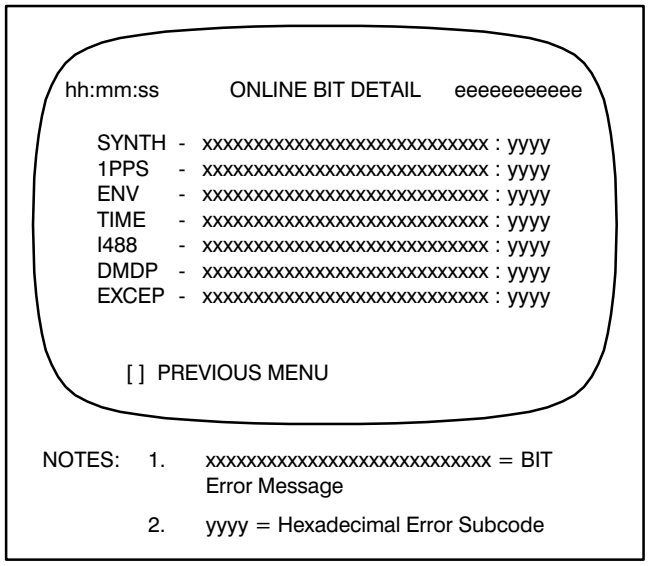


Figure 3 - 12A. Online BIT Detail Display

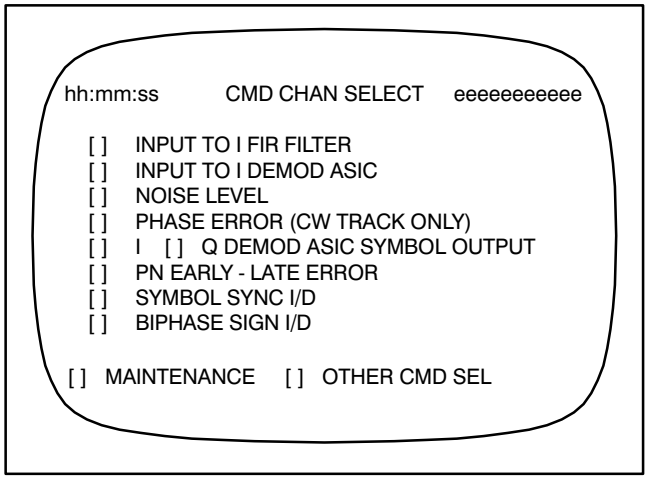


Figure 3 - 14. CMD Channel Test Point Selection Menu 1

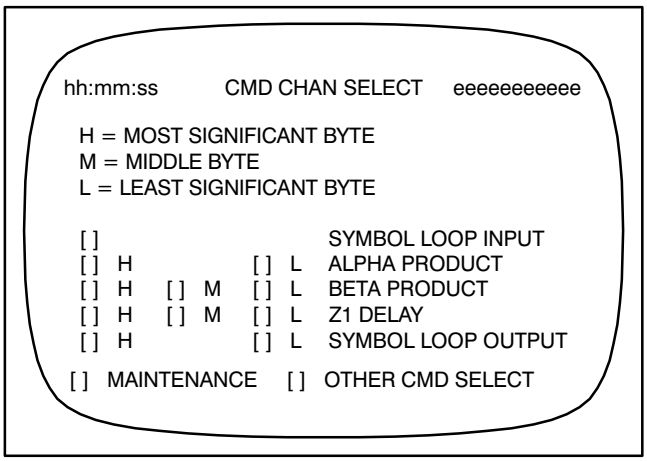


Figure 3 - 15. CMD Channel Test Point Selection Menu 2

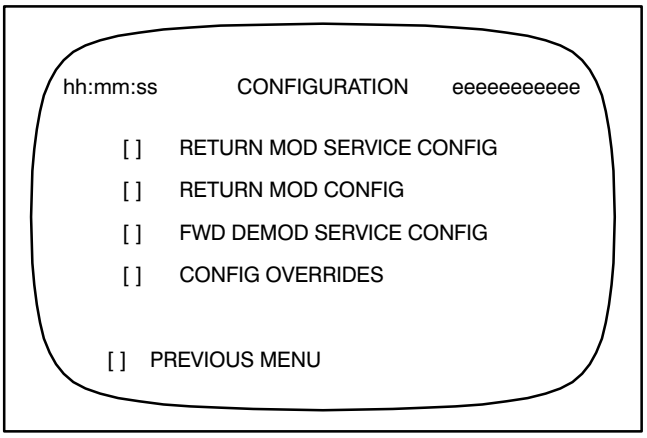


Figure 3 - 16. Configuration Menu

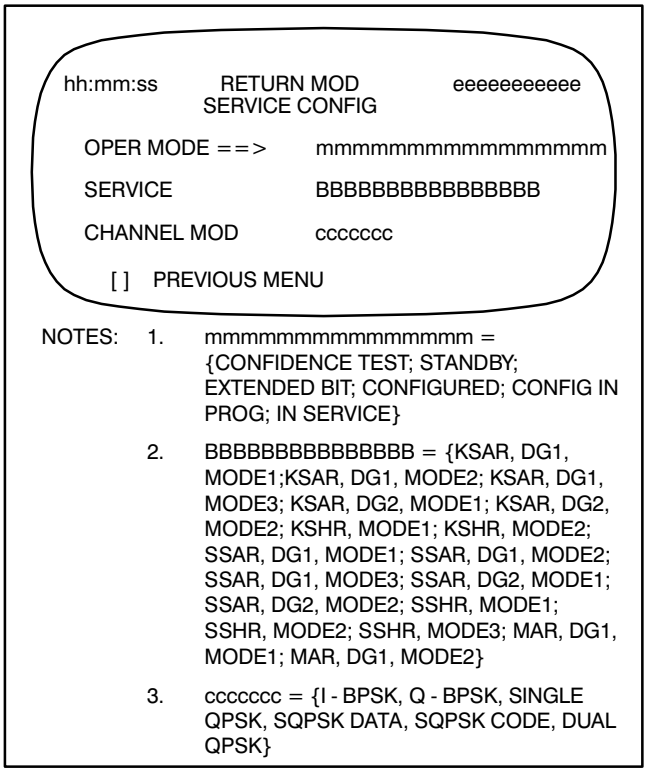


Figure 3 - 17. Return Modulator Service Configuration Display

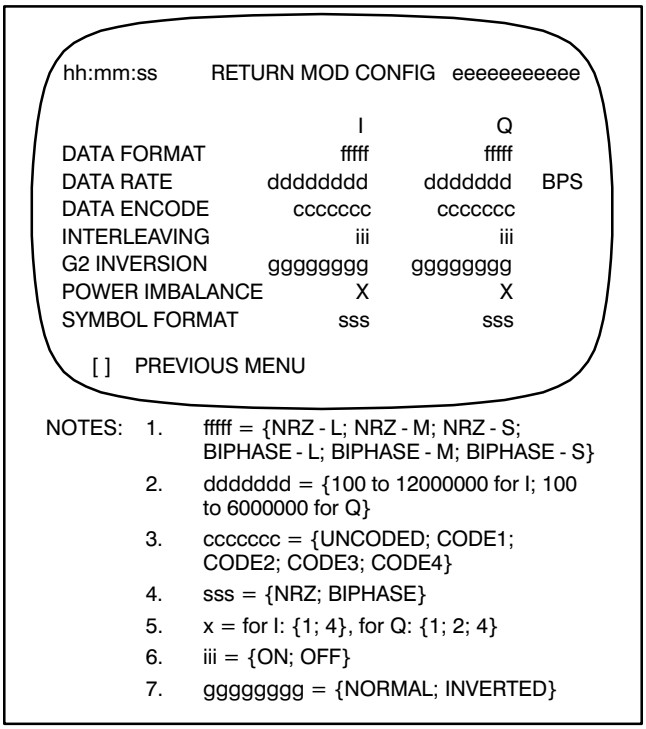


Figure 3 - 18. Return Modulator Configuration Display

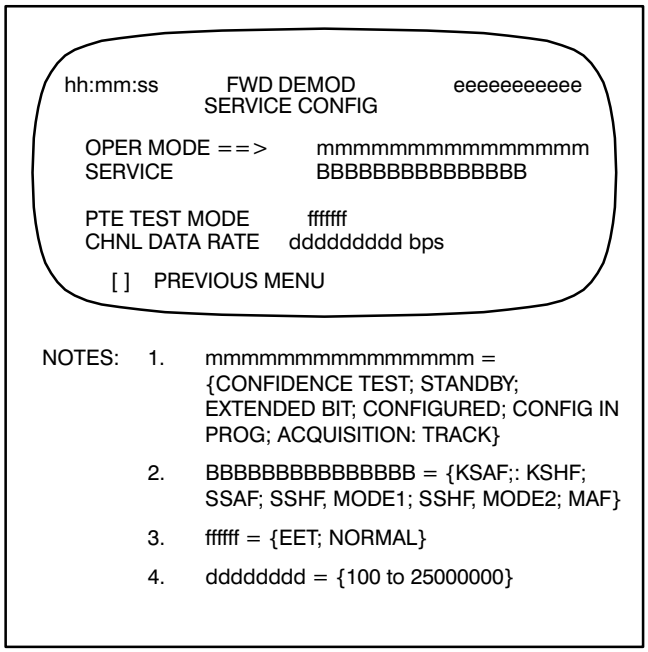


Figure 3 - 19. Forward Demodulator Service Configuration Display

This Page Intentionally Left Blank

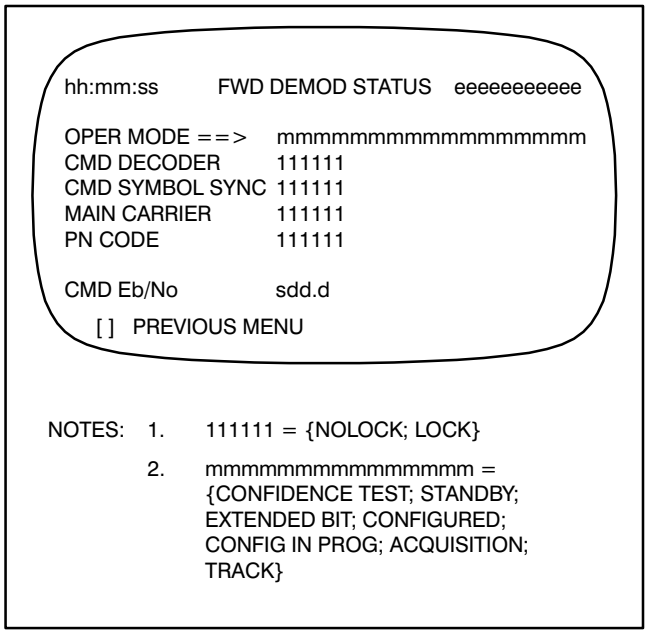


Figure 3 - 20. Return Services Display

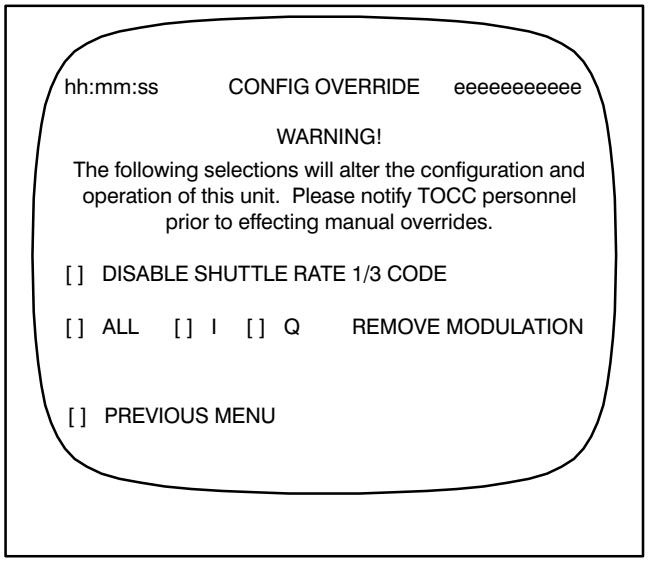


Figure 3 - 21. Configuration Override Display

3–10 Display Error Messages

Table 3-6 contains the possible TM display error messages and descriptions that may occur during operation of the unit.

3–11 Self–Check

Before proceeding with any operation of the TM, refer to paragraph 3-5. The following procedures pertain to operating the TM under local control. Refer to STGT USS TOCC2 operators manual for normal and maintenance operating procedures performed from the TOCC2 console by the TOCC2 operator (remote control). Refer to the applicable O&M manual for maintenance procedures within suspect equipment group, but not accomplished by the TOCC2 operator (performed by the line maintenance technician (LMT) utilizing the maintenance test group (MTG)). The applicable STGT manual numbers and titles are:

a. MA Forward O&M Manual; 530-STGT-O4006.

b. MA Return O&M Manual; 530-STGT-O4005

c. SSA Forward O&M Manual; 530-STGT-O4002.

d. KSA Forward O&M Manual; 530-STGT-O4004.

3–12 Turn–On

The TM requires no special actions to be taken when turning on a newly installed TM assembly. Turn on the TM by placing the ON/OFF switch to the ON position. Verify the AC POWER and DC POWER indicators turn on and the SELECT MENU appears.

3–13 Built–In Test

3–13.1 The TM employs three levels of self-check built-in test (BIT) features. The first-level BIT (confidence BIT) is performed at powerup and reset of the unit (see paragraph 3-18). The second-level BIT (online BIT) is performed continuously during all operational states of the TM (see paragraph 3-19). The third-level BIT (extended BIT) is performed upon command (from ADPE during remote control or front-panel display (EXTENDED BIT SUMMARY MENU; (figure 3-7)) during local control (see paragraph 3-20).

Table 3 - 6. Display Error Messages	
ERROR MESSAGES	DESCRIPTION
INVALID SEL	Notifies the operator that an illegal area on the front panel display was touched; Processing continues awaiting legal operator interaction
NOT LOCAL	Notifies the operator that front panel initiation of the extended BIT function occurred while the Test Modem was in the remote mode; Processing continues awaiting legal operator interaction
BIT RUNNING	Notifies the operator that the BIT function is presently executing and Test Modem operations are halted until completion of the BIT function

3–13.2 During remote control, extended BIT can be commanded during any TM operational state. Refer to section 5, paragraph 5-6 for procedures concerning initiation of TM BIT functions while in the local control condition. Refer to STGT USS TOCC2 operators manual for initiation of TM BIT functions while in the remote control condition.

3–14 Normal Operation

Refer to STGT USS TOCC2 operators manual and TOCC2 operator for operating the TM during normal (remote control) conditions.

3–15 Emergency Operation

Refer to STGT USS TOCC2 operators manual and TOCC2 operator for operating the TM during emergency conditions.

3–16 Shutdown

Secure the TM by placing the ON/OFF switch in the OFF position. Verify the AC POWER and DC POWER indicators turn off.

3–17 BIT Features

The TM employs three levels of BIT features. Refer to the following paragraphs for explanations of the specific functions performed:

a. Confidence BIT: 3-18.

b. Online BIT: 3-19.

c. Extended BIT: 3-20.

3–18 Confidence Bit

The TM runs initialization and self-test routines (confidence BIT) at powerup or unit reset. Upon initiation of the confidence BIT, the front panel TEST indicator is turned on. If any routine does not complete successfully, the FAILURE indicator is turned on and the TM halts operation and/or sets the applicable LRU fail status. Upon successful completion of the confidence BIT, the TEST indicator is turned off, and the TM enters the standby state. The routines are as follows:

a. System random access memory (RAM) test.

b. Central processing unit (CPU) test.

c. Kernel initialization.

d. Interrupt initialization

e. MIL-STD-1553 test.

f. I/O initialization.

g. VME test.

h. DMDP test.

i. Demod application specific integrated circuit (ASIC) test.

j. Environment test.

k. Indicators test.

3–18.1 RAM Test

This test performs four different write, read, and compare operations on the MCP RAM. The RAM test uses a 5's pattern, an A's pattern, an address pattern, and inverse address pattern to determine the RAM health. If any RAM locations fail the front panel FAULT LED is turned on, the status register is loaded with a RAM fail indication, and processing is halted.

3–18.2 CPU Test

This test performs four different tests on the MC68030 CPU resident on the MCP PWA. The first test verifies operation of the CPU data, address, and control registers. The second test verifies operation of the CPU's instruction set. The third test verifies operation of the CPU addressing modes. The fourth test verifies operation of CPU exception processing, including the following exceptions: bus error, address error, illegal instruction, zero division, check instruction, TRAPV instruction, privilege violation, trace, trace on change, line-A emulation, line-F emulation, format error, and the 16 software traps. If any CPU test fails, the front panel FAULT LED is turned on, the status register is loaded with a CPU fail indication, and processing is halted.

3–18.3 Kernel Initialization

This function creates the kernel system environment using the values supplied in the kernel configuration table. Once the kernel pointers have been set up, the kernel workspace is set up, the task control blocks are created, the user stacks are set up, the interrupt service routine (ISR) stacks are created, and the internal kernel variables are initialized. If any of the kernel initialization tasks fail, the front panel FAULT LED is turned on, the status register is loaded with a start-fail indication, and processing is halted.

3–18.4 Interrupt Initialization

This function initializes the interrupt circuitry to allow hardware interrupts to the MCP. All device generated interrupt vectors and autovectors are initialized in the exception vector table during this routine. If any of the interrupt initialization tasks fail, the front panel FAULT LED is turned on, the status register is loaded with a start-fail indication, and processing is halted.

3–18.5 MIL–STD–1553 Test

This function verifies operation of a DDC bus-61553 MIL-STD-1553 device. Tested features include buffer RAM, device configurability, and data transmission/reception in an internal loopback mode. The buffer RAM test writes, reads, and compares 5's, A's, address, and inverse address test patterns. The device configurability test writes, reads, and compares a configuration test pattern to the registers and then resets the registers and reads their reset value. The loopback test sets up the TIME 1 and 2 for 1553 operation, loads test data messages, and instructs the 1553 device to transmit the data. If the data does not transmit correctly or during a specified time, the front panel FAULT LED is turned on and the status register is loaded with a start-fail indication.

3–18.6 I/O Initialization

This function initializes the MIL-STD-1553 remote terminals and RS-232C device to a known state and verifies that state. If any of the I/O initialization tasks fail, the front panel FAULT LED is turned on and the status register is loaded with a start-fail indication.

3–18.7 VME Test

This function verifies proper operation of the PNP, TIME, ACQR, EXCS, TDIF, I488, and DMDP VME data transfer bus. A test data word is written to and/or read from each of the testable PWAs. If a bus exception occurs during access, the test fails. On the PWAs that have read/write capabilities, a test word is written to the PWA, read back from it, then compared to the expected word. If the words do not compare, the VME bus test fails. Processing continues regardless of outcome. The FAULT indicator is turned on if the test failed and status can be determined via the CONFIDENCE TEST RESULTS DISPLAY (figure 3-11).

3–18.8 DMDP Test

3–18.8.1 This function performs two independent tests on the DMDP. The first test is an internal self-test feature and the second is testing the DMDP resident RAM. The self test is controlled by the DMDP TMS processor and verifies operation of itself, FFT device, and operation of the DMDP RAM. The TMS functions tested are: internal register operation, addressing modes, instruction set operation, interrupt processing, and interrupt of the MCP.

3–18.8.2 The second test is called the TMS/MCP dual ported RAM (DPRAM) test. The DPRAM is tested by four write/read data patterns: 5's, A's, address, and inverse address. The 5's and address patterns are written by the MCP and read/validated by the TMS. The A's and inverse address patterns are written by the TMS and read/validated by the MCP. This test fails if any test data read from the DPRAM does not correspond to the test data written to the DPRAM. Processing continues regardless of outcome. The FAULT indicator is turned on if the test failed and status can be determined via the CONFIDENCE TEST RESULTS DISPLAY (figure 3-11).

3–18.9 Demod ASIC Test

This function performs an ASIC signature test. The MCP commands the DMDP to perform an ASIC signature test and then waits for a timeout. If the DMDP responds incorrectly, the DMDP is flagged as faulty and the test is stopped but processing continues. Next the MCP evaluates the result of the signature test. Incorrect test results flag the DMSS at faulty. Processing continues regardless of outcome. The FAULT indicator is turned on if the test failed and status can be determined via the CONFIDENCE TEST RESULTS DISPLAY (figure 3-11).

3–18.10 Environment Test

This function verifies proper operation of the TIME PWA's analog-to-digital (A/D) converter and proper voltage and temperature levels. The TIME status register is read for proper bit settings. If the WRAM bit is not set the test fails. With the WRAM bit set, the test reads the TIME digitized voltage values for 5 Vdc, RF 5 Vdc, 12 Vdc, 15 Vdc, and the unit temperature. If any of these environmental parameters are not within their specified normal ranges, the test fails. Processing continues regardless of outcome. The FAULT indicator is turned on if the test failed and status can be determined via the CONFIDENCE TEST RESULTS DISPLAY (figure 3-11).

3–18.11 Indicators Test

This function verifies proper indicator operation by turning all VMEbus-controlled indicators on for one second. Verification of proper operation is by visual inspection of the indicators while they are turned on.

3–19 Online Bit

Online BIT is a function of the schedule 1-second tasks. Online BIT is run as a continuous process, once per second, during all active TM states. The routines are as follows:

a. Monitor CPU exceptions.

b. Monitor time.

c. Monitor environment.

d. Monitor synthesizer lock.

e. Monitor TMS Status

f. Monitor 1 PPS.

g. Monitor automatic level control (ALC) levels.

h. Monitor IEEE-488.

3–19.1 Monitor CPU Exceptions

This function continually monitors any unexpected CPU exceptions which would set an MCP LRU failure, RS-232 channel 1 or 2 error status/ spurious interrupt that would set an MCP LRU failure, and the 1553 bus channel 1 or 1553 channel 2 error status/spurious interrupt that would set a TIME DEMOD or TIME MOD LRU failure, respectively. The FAULT indicator is turned on if a failure occurs. Processing continues

regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3–19.2 Monitor Time

This function monitors the 1-second, 100-millisecond, 10-millisecond, and 1-millisecond interrupts and compares them to relative nominal values. If this value varies by more than one count, the TIME1 (TIME DEMOD) LRU is flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3–19.3 Monitor Environment

This function verifies proper operation of the TIME1 PWA's A/D converter (ADC) and proper voltage and temperature levels. The TIME1 (TIME DEMOD) status register is read for proper bit settings. If the WRAM bit is not set the test fails. With the WRAM bit set, the test reads the TIME1 digitized voltage values for 5 Vdc, RF 5 Vdc, 12 Vdc, 15 Vdc, and the unit temperature. If any of these environmental parameters are not within their specified normal ranges, the test fails and the suspect LRU is flagged (TIME DEMOD, 5V, RF5V, 12V, 15V, or Temp). The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3–19.4 Monitor Synthesizer Lock

This function checks the Reference 10-MHz bit for assertion and either of the 140-MHz or 61.5-MHz bits for non-assertion on the TIME1 (TIME DEMOD) for SYNTH1 (SYNTH DEMOD) and TIME2 (TIME MOD) for SYNTH2 (SYNTH MOD). Any of these conditions cause the respective SYNTH LRU to be flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3–19.5 Monitor TMS Status

This function checks the status of the TMS/MCP interface by sampling the DMDP Time Tag Error bit for a true setting or that the DMDP Command Rejection Count register value is not zero. Next, the unit state and TMS operational mode are used to set up a two dimensional state validation matrix and then compared. Two consecutive inconsistent comparisons set a fault flag. Any of these fault conditions cause the DMDP LRU to be flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3–19.6 Monitor 1 PPS

This function samples the Synchronization Complete bit and the Synchronization Error bit for a true setting. This condition causes the TIME1 (TIME DEMOD) LRU to be flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3–19.7 Monitor ALC Levels

This function monitors the ALC signal levels to detect a modulator (TMOD) LRU failure. The ALC signal levels are digitized via the TIME1 (TIME DEMOD) ADCs and compared with nominal values. Any level not within specified range causes the TMOD LRU to be flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3–19.8 Monitor IEEE–488

This function monitors the status of the IEEE-488 instruments and controller to detect instrument or controller failure. Any status indicating a failure flags its respective LRU (I488, Eb/No, BERTC, BERTI, or BERTQ) as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3−20 Extended Bit

The extended BIT is executed only upon command via the 1553 bus interface (remote control) or front panel (local control). While extended BIT is in progress, all other TM functions, except those which maintain time, are paused. Upon completion of extended BIT, the unit returns to the standby state. The extended BIT routines are broken up into five groups; group 1 is the basic functions test (tests 1 through 6), group 2 is the receiver functions test (tests 7 and 8), group 3 is the modulator functions test (test 9; TDIF test), group 4 is the I488 functions test (tests 10 and 11), and group 5 is the RF loopback test (test 12). The basic functions test routines are as follows:

a. MCP Test (Test 1).

b. VME Test (Test 2).

c. TIME Test (Test 3).

d. DMDP Test (Test 4).

e. Demod ASIC Test (Test 5).

f. Signal Level Test (Test 6).

The receiver functions test routines are as follows:

g. PNP Test (Test 7).

h. Correlator Tap Test (Test 8).

The I488 functions test routines are as follows:

i. I488 Controller Test (Test 10).

j. I488 Instruments Test (Test 11).

3−20.1 MCP Test

3−20.1.1 The MCP test passes if both subtests pass; the 68030 subtest and programmable interval timer (PIT) subtest. The 68030 subtest performs four different tests on the MC68030 CPU. The first test verifies operation of the CPU data, address, and control registers. The second test verifies operation of the CPU's instruction set. The third test verifies operation of the CPU addressing modes. The fourth test verifies operation of CPU exception processing.

3−20.1.2 The second subtest verifies operation of the two MCP PITs. This subtest tests the PITs' registers, timers, and interrupts. The registers are tested by writing and reading a test word to/from each register and verifying that the word read from the register is the same as the word written to the register. The two PIT timers are tested by comparing their measurement of a short period of time. This subtest fails if a register data write/read is inconsistent, or if the PIT timers do not measure a period of time within +/- 5% of each other, or if the PIT interrupts do not occur. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 1) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3−20.2 VME Test

The VME test verifies operation of the VME data transfer bus. A test data word is written to and/or read from each of the applicable VME slave LRUs (PNP, ACQR, TIME1, TIME2, I488, EXCS, TDIF, and DMDP). If a bus exception occurs during LRU access, this test fails. On those LRUs that have a write/read capability, a test word is written to the LRU and then compared to the test word read from that LRU. If the test data words do not compare, this VME bus test fails. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 2) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3−20.3 Time Test

The TIME test performs two independent tests on the TIME PWA. The first test verifies that the four timing interrupts (1, 20, 100, and 1000 pps) occur within a specified tolerance. The second test verifies that the 6.2 Vdc reference signal is within a specified tolerance. The intervals of the timing interrupts are measured by a PIT counter and the 6.2 Vdc reference input to the TIME A/D converter is converted to a digital representation and verified. Also, if resynchronization is in progress and no external 1-PPS signal is present, this test will fail due to a lack of time interrupts. The FAULT

indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 3) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.4 DMDP Test

3–20.4.1 The DMDP test performs two independent tests on the DMDP. The first test is an internal self-test feature and the second tests the DMDP resident RAM. The self test is controlled by the DMDP TMS processor and verifies operation of itself, FFT device, and operation of the resident RAM. The TMS functions tested are, internal register operation, addressing modes, instruction set operation, interrupt processing, and interrupt of the MCP.

3–20.4.2 The second test is called the TMS/MCP dual ported RAM (DPRAM) test. The DPRAM is tested by four write/read data patterns: 5's, A's, address, and inverse address. The 5's and address patterns are written by the MCP and read/validated by the TMS. The A's and inverse address patterns are written by the TMS and read/validated by the MCP. This test fails if any test data read from the DPRAM does not correspond to the test data written to the DPRAM. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 4) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.5 Demod ASIC Test

This test performs an ASIC signature test. The MCP commands the DMDP to perform an ASIC signature test and then waits for a timeout. If the DMDP responds incorrectly, the DMDP is flagged as faulty and the test is stopped but processing continues. Next the MCP evaluates the result of the signature test. Incorrect test results flag the DMSS as faulty. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 5) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.6 Signal Levels Test

The signal levels test verifies that a dc bias can be compensated for, and that the RMS I and Q signal levels are within +/- 5% of each other, when measuring a test signal. This test verifies the signal levels through three data paths in the TM. The MCP selects a 70-MHz test signal and commands the TMS processor to perform a dc bias procedure. The MCP then verifies that the new bias values have not varied more than a specified tolerance amount from their previous values. The MCP then configures the TMS processor for a carrier NCO offset of 10 kHz from its 8.5-MHz frequency, with a sample rate of 5-Hz bin width. The MCP commands the TMS processor to acquire and after acquisition is achieved, reads the RMS magnitude of the I and Q signals from the TMS processor. The I and Q signal magnitudes are compared by the MCP to determine test results as defined above. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 6) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.7 PNP Test

This test configures the PNP to generate PN codes, and cause an interrupt at epoch occurrence. The PN codes at the epoch are sampled to verify their values. Acquisition and track epoch interrupts are timed to verify that they occur within a specified tolerance time interval. If any sampled PN codes are not as expected, or if an epoch interrupt does not occur or occurs outside of the tolerance, the test fails. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 7) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.8 Correlator Tap Test

3–20.8.1 This test configures the PNP with values of coherent and non-coherent signal combination parameters and NCO parameters. The ACQR is configured with an offset (Z), correlator MUX set to select a constant “1”, and the following correlator lengths:

Correlator Length (A)	Corresponding Taps and Bin Magnitudes
00h	4
55h	344
AAh	684
FFh	1024

3–20.8.2 The correlator tap test passes if each of four selected taps yield expected peak indices and bin magnitudes, and if a peak detect interrupt occurs within a specified period of time. Unexpected peak indices, bin magnitudes or peak detect interrupts cause the test to fail. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 8) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.9 Modulator Functions Test

This TDIF test configures the TDIF LRU to generate PN codes, and cause an interrupt at epoch occurrence. The PN codes at the epoch are sampled to verify their values. Acquisition and Track epoch interrupts are sampled to verify that they occur within a specified time interval. If any sampled PN codes are not as expected, or if an epoch interrupt does not occur or occurs outside of the time intervals, the test fails. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 9) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.10 I488 Controller Test

This I488 test passes only if all tested functions of the IEEE-488 LRU are operating as expected. This test verifies operation of the following functions: I488 reset, I488 DMAC register operation, IEEE-488 controller operation, I488 DMAC error handling, I488 DMAC interrupt generation, I488 DMAC data transfer, and I488 DMAC carry cycle I/O. If any of the tested IEEE-488 LRU functions are not operating as expected, then the test fails. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 10) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.11 I488 Instruments Test

This I488 test verifies that each instrument does not indicate a failure condition either before or after self-test or configuration processing. If any of the IEEE-488 instruments do not pass their built-in self-tests or cannot be configured without an error occurring, then the test fails. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 11) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.12 RF Loopback Test

This test configures TM into a closed loop mode. The TDIF and PNP code generators are set to the same code and the TMOD output and RFDC input set to the same frequency. This test fails if the receiver section of TM is unable to acquire and track the transmitted signal or if the received signal or bit error rate is not within prescribed ranges. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 12) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

Section 4 - Theory of Operation

4 - 1 Introduction

This section provides a functional description of the Test Modem (TM). A general functional description is presented at the block diagram level, followed by individual detailed descriptions of the unit's major functions and hardware/firmware components. The detailed descriptions are supported by timing, flow, logic, and schematic diagrams, when necessary. The information contained in this section is keyed to the Level 1 maintenance procedures in section 5.

4 - 2 Detailed Functional Description

The TM processes all SSA, MA, KSA low data rate forward/return data for the STGT USS in support of pre-service, post-maintenance, and end-to-end test verification of associated USS Integrated Receiver and Modulator/Doppler Predictor equipment configurations. Having the capability of supporting each of these configurations (SSA, MA, and KSA), TM can be used interchangeably in any of the unique equipment groups. Although TM supports the above mentioned configurations, not all of TM's functional capabilities are required for each. Refer to figure 4-1 for the following general functional description.

4 - 3 Firmware Descriptions

The TM contains three distinct firmware programs: the executive program (Exec), the TM program, and the DMDP program. The TM and DMDP programs are application programs that provide the necessary scheduling and control of the TM during operation. The executive program provides I/O services for the TM application program.

4 - 3.1 Executive Program

The Exec provides the application programs with a real-time operating system. The operating system provides multi-tasking and resource management of unit input/output. Part of the Exec consists of the VRTX32 multi-tasking kernel that provides the multi-tasking scheduling and memory resource management functions. The Exec is comprised of the following function design units (FDUs) and together combine to provide an integrated interface between the hardware and the application programs:

a. Power-On and Exec Initialization. This FDU is started by either a hardware reset or an application call execute command (Excmd) to reinitialize. When this occurs, this FDU checks the system RAM, boots all code into the system RAM and then starts operation from system RAM. The system kernel is initialized, the event vector table is setup, and I/O devices are initialized. Finally, the I/O devices are tested as part of the online BIT FDU and the application program is started.

b. Input/output. I/O FDUs (RS-232 and MIL-STD-1553) typically have two entry points that consist of functions that the applications call (i.e. Exec Read and Exec Write) and interrupt service routines (ISRs) that are invoked by the hardware generated interrupts. The application programs use the I/O FDUs to interface to the system I/O hardware.

c. Event Handlers. This FDU provides the interrupt service routines for the signal processing and timing hardware interrupts that schedule the time critical signal processing.

d. Exception Handlers. This FDU interfaces the MC68030 to error processing and recovery ISRs. These ISRs also allow for report generation that details the error that was encountered.

e. Download Code. This FDU provides the capability of downloading software code to the MCP processor. Ephemeris data download is also included in this FDU. The download is via the MIL-STD-1553 bus.

f. Exec BIT. This FDU provides confidence tests for the I/O devices that can be called by the power-on and Exec initialization FDU or by the application program.

4 - 3.2 TM Program

The TM program is the master application program of the TM. The TM program's purpose is to configure and control the TM in providing test signals required to support pre-service verification of associated USS IR and MDP units. The TM provides necessary return data signals and receives forward signals, and has the capability to provide simulation of coherent forward/return services. It also provides status updates to the ADPE via the MIL-STD-1553 bus interface. The TM is remotely controlled via the 1553 bus interface and as the master program, provides any data required by the DMDP processor. The TM program also interfaces with TIME1 & 2, the front panel (via an RS-232 interface), PNP, I488, EXCS, TDIF, and ACQR. The TM program is comprised of the following functions:

a. Command Processor Function. The command processor function processes the commands received over either of the 1553 bus interfaces and determines whether the command applies to the return or forward test portion of the TM. Commands over the 1553 bus interface are asynchronous and this function processes each command upon receipt. Some commands contain an effective time of when the action defined within the command is to take place. On startup, this function clears the 1553 bus interface and initiates input from the 1553 bus interface and processes that input. Verification is made that the LOCAL/REMOTE switch is in the REMOTE position and the TM is in a valid operating mode before processing any commands. When applicable, the ephemeris database is updated. This function is capable of filling the database to its maximum size of 50 minutes with a limit of 10 minutes of ephemeris per transfer.

b. PN Controller Function. The PN controller function controls all aspects of the PNP and ACQR operation. Upon a Demod Configuration command, the ACQR and PNP configurations are updated. Next, PN acquisition is begun upon receipt of a Start Acquisition command. During the PN acquisition, this function searches the range of code and Doppler uncertainty and provides code offsets and Doppler estimates to the DMDP. PN acquisition is performed in parallel with the DMDP's carrier acquisition process until the DMDP indicates frequency lock.

   Upon frequency lock, this function indicates PN lock and begins to update the open ended code loop until a timeout occurs, at which time, it will transition to track; otherwise, the search process continues. The open loop track process uses the Doppler value that was found during the DMDP's fast fourier transform (FFT) search to update the track code NCO. Once processing transitions to track, the track NCO is updated every 10 milliseconds using a 2nd-order tracking loop. This loop is aided with the DMDP's measured carrier Doppler valued in all modes except SSH mode. If a phase loss-of-lock occurs, the TM remains in the track state.

c. Demod Controller Function. The demodulator controller function controls all data transfers between the MCP and the DMDP. This function sends a Perform DC Bias command to initialize DMDP to a known state and verifies the DMDP's operating mode status as standby. All commands to the DMDP are sent asynchronously with a semaphore scheme that allows only one command to be processed at a time. Next, the DMDP is configured.

   During carrier acquisition, the DMDP interrupts the MCP when the carrier has been acquired. When this occurs, this function notifies the PN controller function to enter PN open-loop track (spread modes only) and to use the Doppler offset that the DMDP found during the FFT search for both the code and pre-correction NCOs. Once every 10 milliseconds, the DMDP sends its status to the MCP. All lock bits are monitored for lock during the entire 1-second period and if any 10-millisecond status report shows a loss of lock, that entire 1-second period is reported as no lock. This function also resolves channel ambiguity.

d. Ephemeris Processing Function. This function performs carrier Doppler pre-correction on the forward signal by controlling the TIME NCO based on receiver Doppler ephemeris and FFT Doppler offset from the DMDP. This

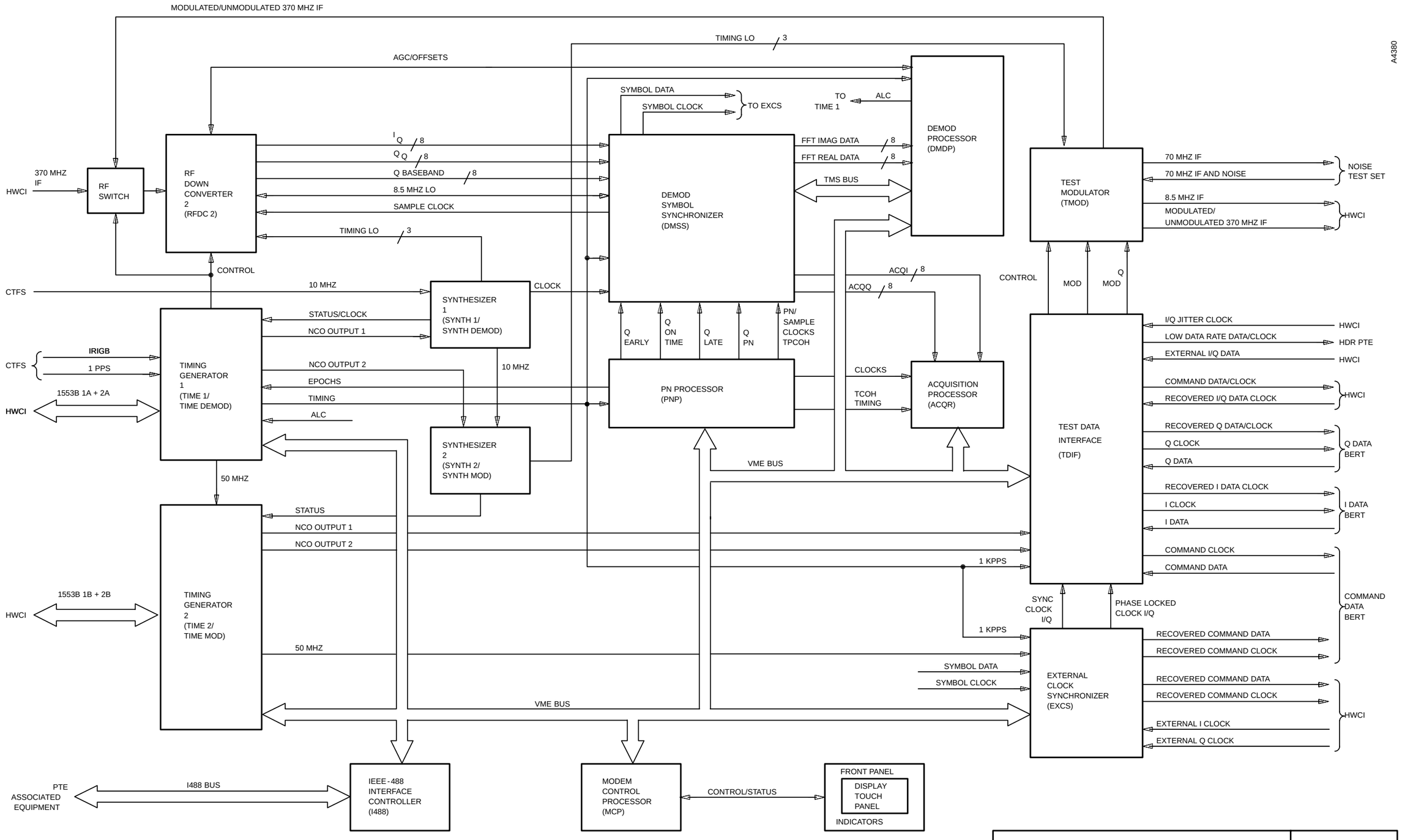


FIGURE 4-1. TEST MODEM FUNCTIONAL BLOCK DIAGRAM

4-3/4-4

NCO is updated every two milliseconds. Also, this function generates the forward (modeled) code state based on the Doppler profile in the receiver ephemeris every two milliseconds. This function starts the code generation at the 1 PPS of the service start time. The output of this function is used by the select search interval function.

e. Time Management Function. This function maintains time-of-year (TOY) and various timers that are used throughout the TM. The TOY is updated once a second with a resolution of one millisecond. The phased-lock timer is zeroed upon receipt of a carrier frequency acquisition event and incremented until the DMDP enters carrier phased-lock with a resolution of 10 milliseconds.

f. Interactive Touch Panel Controller Function. This function processes the touch panel entries received from the display and updates the display based on those entries.

g. Test Modulator Controller Function. This function is responsible for the modulator portion of the TM. Upon a configuration command, the TDIF PN code RAM is loaded, and the following modulator characteristics are set: I & Q data encoding, I & Q data interleaving, spread/non-spread modes, I & Q data clock rates, power ratio, and single/dual channel operation. Next, the PN code is started by loading the PN generators with a code state value of zero so that the master PN epoch occurs at the service start time. When coherent turnaround is selected, the PN generators are loaded with the recovered code state so that the return signal epoch is time aligned with the recovered forward epoch (spread modes only). The Doppler for the carrier and PN code signals based on the Doppler profile is provided in the ephemeris.

h. Instrument Controller Function. This function initializes all instruments on the IEEE-488 bus interface and verifies they are online and set to a known state. This includes calibrating the noise test set attenuator on the TMOD PWA in order to implement commanded negative carrier-to-noise ratios. The instruments are configured and upon start operation, the BER and TIC measurements are updated.

i. Performance Monitor Function. This function consists of the online BIT, extended BIT, confidence BIT, manage fault light, and prepare status reports. Refer to section 3 for explanations of the BITs and manage fault light functions. The prepare status reports function examines status and data from all major data sources and converts the information into the appropriate status report format. All reports are available to be read by the 1553 bus interface at the 400-millisecond mark after each 1 PPS. The reports consist of the following: modulator configuration report, demodulator configuration report, modulator performance report, demodulator performance report, general configuration report, extended BIT report, and BER/TIC measurement report.

4 - 3.3 DMDP Program

The DMDP program provides frequency acquisition, data tracking, and real-time demodulator control in the TM. The DMDP is under the control of the MCP but the actual processing flow is a function of external inputs from the peripheral hardware. The DMDP program receives command and configuration data from the MCP and DMDP processing status is sent to the MCP. The DMDP program is comprised of the following functions:

a. Interpret Commands. The MCP to DMDP interface uses a semaphore scheme that allows only one command to be processed at a time. The DMDP program notifies the MCP when it has finished processing a command. Valid commands are passed on to the system. Invalid commands are ignored. The possible commands are: reset TMS, perform dc bias, BIT, configure, start acquisition, Doppler estimate, and initialize.

b. Configure Demodulator. This process upon power-up reset will: copy the firmware program from PROM to RAM, set up configuration data area to a known default configuration, and proceed with the configuration process. For a Configuration command, this function sets up the firmware and hardware as per the configuration data which is either: the default configuration or downloaded initial configuration command data from the MCP

(the MCP also downloads auxiliary configuration data for use in subsequent processing stages). Complete configuration is performed within 20 milliseconds.

c. Signal Processing. This function provides the frequency acquisition and data tracking capabilities for the TMS. This function includes the following subfunctions: acquire the carrier, track the carrier, noncoherent AGC, coherent AGC, compile the DMDP status, track the data, update configuration, and estimate RMS noise. The acquire-the-carrier function provides the FFT processing to search for the carrier over a range of Doppler uncertainty. Track the carrier provides the phased-lock loop tracking function for carrier, subcarrier and recovered carrier. Noncoherent AGC provides carrier lock status based on the input signal power and the phase error. Both lock and loss-of-lock condition are monitored. Coherent AGC adjusts and maintains constant signal levels to the decoder and carrier loop functions to optimize their performance. The AGC value is based upon the measured signal magnitude.

   Compile DMDP status function utilizes the semaphore scheme whereby the TMS is allowed to run without queuing up its status data. If TMS has determined that the MCP has not completed its access of the status data then no new status data is written to the interface. Each time the TMS updates status, it increments a counter that is part of that status. The counter allows the MCP to affirm that status is new, but static. Track-the-data function monitors the hardware and carrier-lock status, keeping track of the data tracking peripherals and monitoring for both a lock condition and a loss-of-lock condition. Update configuration provides updated modifications to the demodulator configuration during the processing of a signal. Estimate RMS noise computes an estimate of the RMS noise level for the soft decision circuitry based upon a lookup table.

d. Commanded BIT. Commanded BIT results from the direct command from the MCP and provides status back to the MCP. This BIT supports the following tests: self-contained ASIC BIT and bidirectional memory test of dual port RAM in concurrence with the MCP. Refer to section 3 for further information on these tests.

4 - 4 States of Operation

4 - 4.1 Introduction

4−4.1.1 The TM operating states are described as they pertain to two major operating modes, TM Coherent mode and TM Non-Coherent mode. The TM Non-Coherent mode is the operational mode where the TM modulator and TM demodulator functions are treated as two individual units. The frequency sources (local oscillators) between the modulator and demodulator are independent of each other. This mode is used during preservice testing of forward and return chains, and non-coherent end-to-end test (EET) services. The TM Coherent mode is the operational mode where the TM modulator frequency source is coherently related to the TM demodulator frequency source. This mode is used during coherent EETs.

4−4.1.2 Within the two TM modes, there are three different operating states. In the TM Non-Coherent mode, there are the demodulator receiver states and the modulator states. In the TM Coherent mode, there are the coherent states. The demodulator receiver states pertain to the receiver portion of the TM. The modulator states pertain to the modulator portion of the TM. For the TM Coherent mode, the coherent states describe the state transitions showing the modulator and demodulator integrated and operating as a single unit.

4 - 4.2 Non-Coherent Demodulator States

4−4.2.1 Refer to figure 4-2 for the following demodulator (forward service testing) states discussion. The confidence test in progress state is entered at power-up or reset and the front-panel TEST LED is turned on. During this state, the TM executes its confidence test and does not respond to any 1553 bus communications. This state completes in less than 10 seconds and the TEST LED is turned off. If the confidence test fails, the front panel FAULT LED is turned on and remains on. The extended BIT state is entered by an Extended BIT command over the 1553 bus

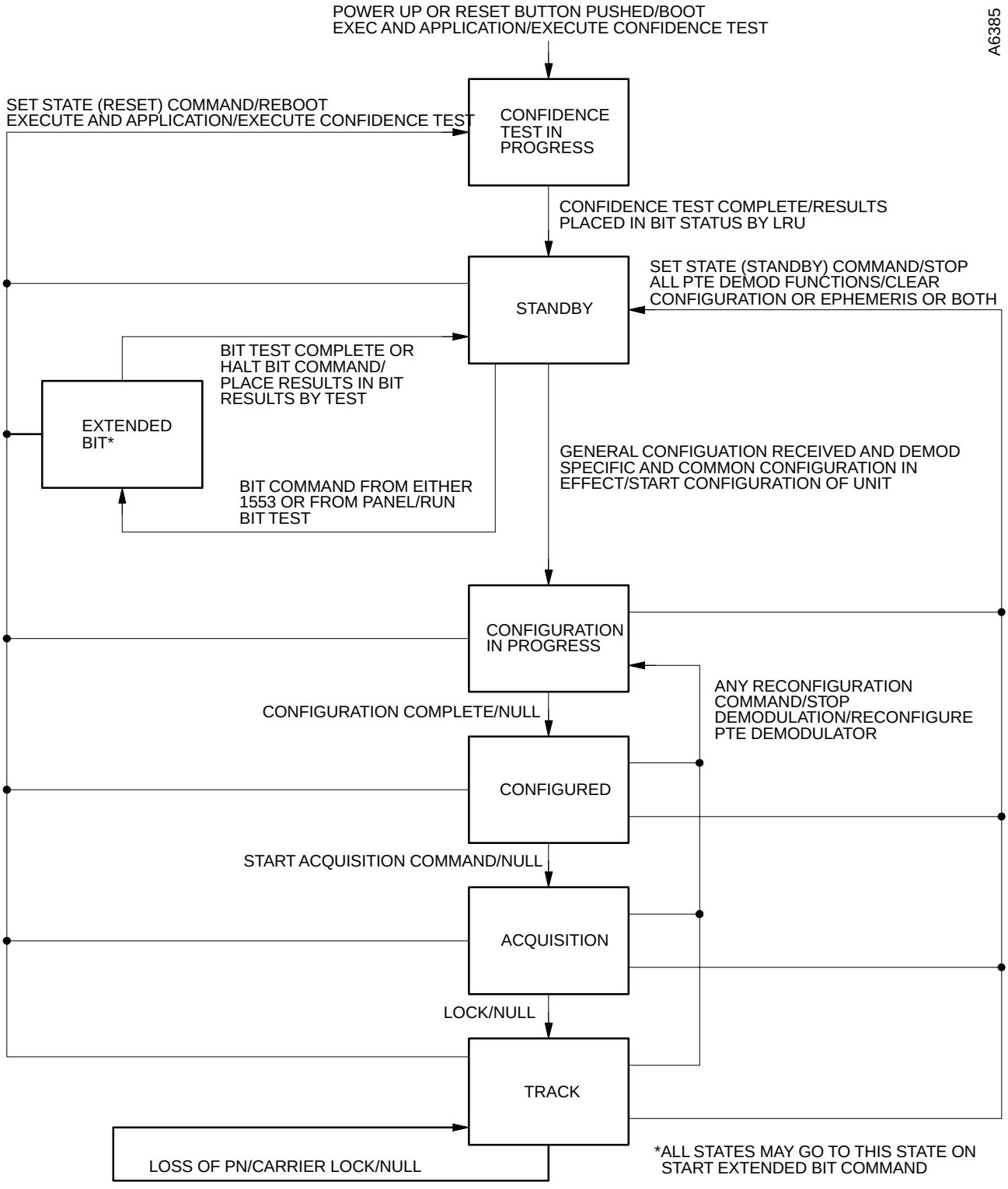


Figure 4 - 2. Non-Coherent Demodulator States

interface (remote) or front panel display (local) and exits upon completion or by termination of the BIT by either front panel or 1553 bus command.

4−4.2.2 The standby state is entered at the completion of the confidence test or by command via the 1553 bus interface while the TM is in one of the other operating states. The standby state indicates that the TM is ready to receive a General, Common, and Specific Configuration command. The General Configuration command specifies whether the modulator frequency source is derived locally or from the demodulator section (demod is specified for end-to-end testing). The Common and Specific Configuration commands are used for initial configuration or reconfiguration of the forward service parameters of the TM demodulator. A General command must be received before the Common and Specific commands are received. Upon receipt of all three configuration commands, the TM enters the configuration in progress state.

4−4.2.3 The demod configuration in progress state indicates that TM is dedicated to the commanded return service configuration of the unit. No other signal acquisition or tracking is done while in this state. Upon completion of initializing all applicable circuits to the configuration, the TM transitions to the demod configured state. This state indicates that the TM is ready to accept a start PN model command and start acquisition command. The start PN model command supplies the forward PN epoch times for spread modes. Start of this command resets all forward control commands in the PN model (such as Doppler control, etc.).

4−4.2.4 Upon receipt of a start acquisition command, the TM begins attempting to acquire the signal as previously configured. Any reconfiguration command during this state transitions the TM to the configuration in progress state. Upon receipt of a carrier/phase lock status, the TM transitions to the tracking state. This state indicates that the TM has achieved lock, and is tracking the signal. This is the only state that the tracking report data is valid. The TM stays in this state until a command requiring a state change is received. While in tracking state, the TM can accept a Demod Range Channel Reacquisition command. This command may be issued during internal loop tests of non-Shuttle services, after acquisition and tracking of the command channel has been achieved. In response to this command, the TM demodulator acquires and tracks the range channel PN code.

4−4.2.5 The Non-Coherent Demodulator mode allows for one other command while in the configured state or tracking state. The command is Start FWD BER Test command and it sets up and initiates BER testing of the forward channel via the CMD BERT test set. In response to this command, the TM automatically detects and corrects for data inversion, and then sets up the CMD BERT for a mode test with BER options selected. This command specifies the test interval (number of bit cycles for each BER measurement) and the test period, which specifies the total test time (normally the service time) of the test to be performed. Test measurements and elapsed time continue during an out-of-sync condition, which is reported as status. Resync is automatically performed by the CMD BERT. The CMD BERT runs the test for the test period specified, and updates its status upon completion of each test interval. Once a BERT test is started, it may be restarted/stopped in the middle of a test by resending this command, with a new set of start/stop parameters.

4 - 4.3 Non-Coherent Modulator States

4−4.3.1 Refer to figure 4-3 for the following Non-Coherent Modulator (return service testing) states discussion. The confidence test in progress state is entered at power-up or reset and the front panel TEST LED is turned on. During this state, the TM executes its confidence test and does not respond to any 1553 bus communications. This state completes in less than 10 seconds and the TEST LED is turned off. If the confidence test fails, the front panel FAULT LED is turned on and remains on. The extended BIT state is entered by an extended BIT command over the 1553 bus interface (remote) or front panel display (local) and exits upon completion or by termination of BIT by either front panel or 1553 bus command.

4−4.3.2 The standby state is entered at the completion of the confidence test or by command via the 1553 bus interface. The standby state indicates that the TM is ready to receive a General and Modulator Configuration command. The General Configuration command specifies whether the modulator frequency source is

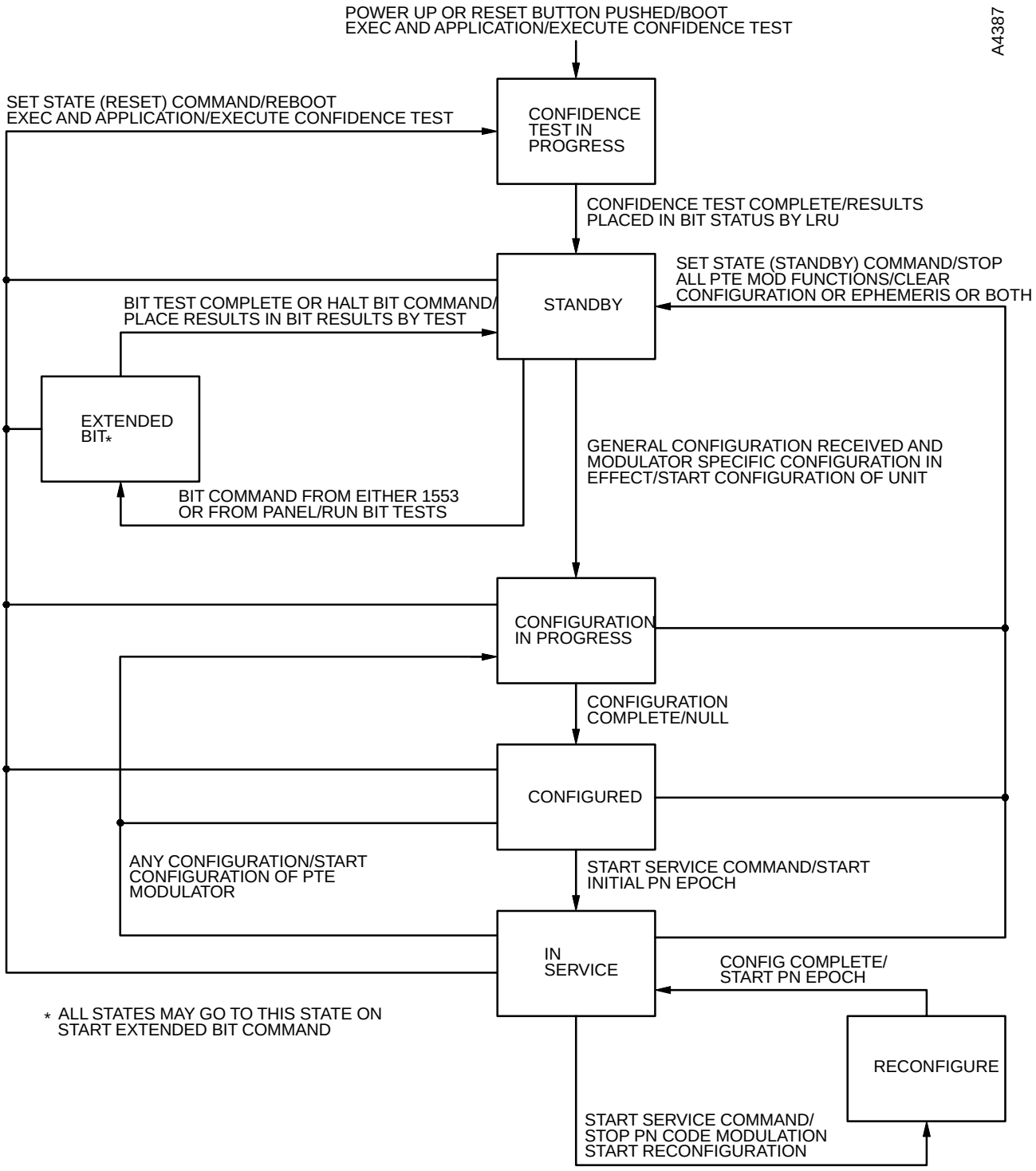


Figure 4 - 3. Non-Coherent Modulator States

derived locally or from the demodulator (demod is specified for end-to-end testing). The Modulator Configuration command is used for initial configuration or reconfiguration of the return service parameters of the TM modulator. A General command must be received before the Modulator Configuration command is received. Upon receipt of both configuration commands, the TM enters the configuration in progress state.

4−4.3.3 The configuration in progress state indicates that the TM is dedicated to the commanded forward service modulator configuration of the unit. Upon completion of initializing all applicable circuits to the configuration, the TM transitions to the configured state. This state indicates that the TM is ready to start the return service modulator output of the signal as specified by the configuration commands. Upon receipt of a Start Service command, the TM enters the modulator in service state. This state indicates that the TM has received the Start Service command and has started the modulation output.

4−4.3.4 The Start RTN BER Test and Measure Time Interval commands can be accepted while the TM is in the configured or modulator in service states. The Measure Time Interval command sets up and initiates time interval testing for return channel data delay of the return I and/or Q channels via the HP 5316B Universal Counter (Time Interval Counter (TIC)). Upon receipt of this command, the TM sets up the TIC for the time interval A to B mode, positive slope trigger. In this mode, the TIC is set up to make a one shot measurement of the delay between the pattern sync transmit pulse and the pattern sync receive pulse of the associated BERTs (I or Q channel BERTs). These sync pulses in the BERTs are square waves which alternate once during each pattern cycle. For the receive pulse to be valid, this measurement must be made only when the BERTs indicate pattern sync. This command provides the counter with the detection voltage trigger level, approximately at the center of the peak-to-peak sync pulse levels.

4−4.3.5 The Start RTN BER Test command sets up and initiates BER testing of the return I and/or Q channels via the PTE I and Q BERTs. Upon receipt of this command, the TM automatically detects and corrects for data inversion, and then sets up the BERTs for test mode with the BER option selected. This command specifies the test interval (number of bit cycles for each BER measurement) and the test period, which specifies the total test time (normally the service time) of the test to be performed. Test measurements and elapsed time continues during an out-of-sync condition, which is reported as status. Resync is automatically performed by the BERTs. Once a BER test is started, it may be restarted/stopped in the middle of a test by resending this command with a new set of start/stop parameters.

4 - 4.4 Coherent Mode States

4−4.4.1 The states described in the Non-Coherent Mode states (demodulator and modulator) are the same definitions as those in the Coherent states. In the TM Coherent mode, these states interact slightly different. Refer to figure 4-4 for the following Coherent Mode states discussion.

4−4.4.2 The confidence test in progress state is entered at power-up or reset and the front panel TEST LED is turned on. During this state, the TM executes its confidence test and does not respond to any 1553 bus communications. This state completes in less than 10 seconds and the TEST LED is turned off. If the confidence test fails, the front panel FAULT LED is turned on and remains on. The extended BIT state is entered by an Extended BIT command over the 1553 bus interface (remote) or front panel display (local) and exits upon completion or by termination of BIT by either front panel or 1553 bus command.

4−4.4.3 The standby state is entered at the completion of the confidence test or by command via the 1553 bus interface. The standby state indicates that the TM is ready to receive a General, Modulator Configuration, Demod Common, or Demod Specific Configuration command. The General Configuration command specifies whether the modulator frequency source is derived locally or from the demodulator (demod is specified for end-to-end testing (coherent mode)). The Demod Common and Demod Specific Configuration commands are used for initial configuration or reconfiguration of the forward service parameters of the TM demodulator. The Modulator Configuration command is used for initial configuration or reconfiguration of the return

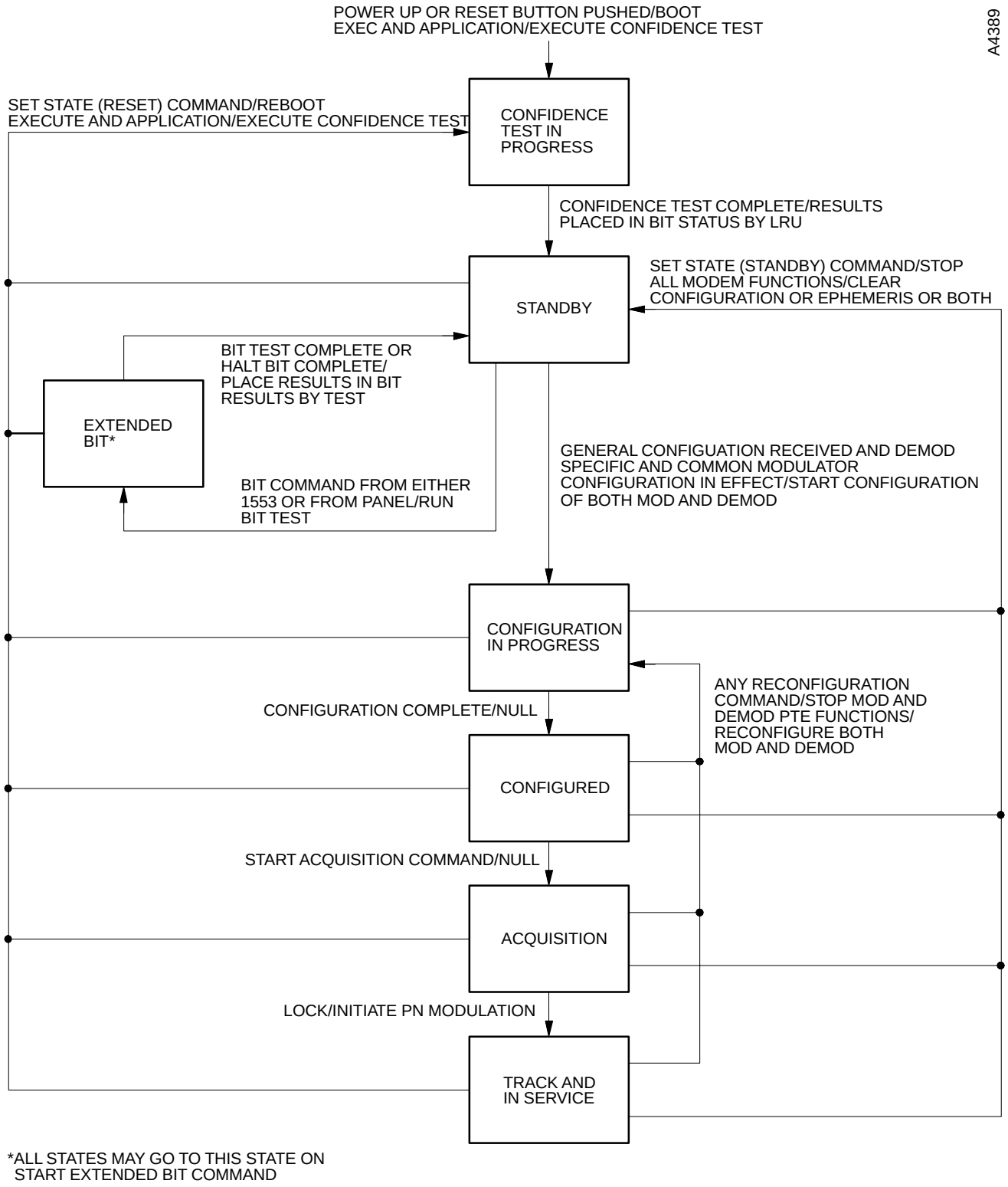


Figure 4 - 4. Coherent Modulator/Demodulator States

service parameters of the TM modulator. A General command must be received before the Modulator, Demod Common, and Demod Specific commands are received.

4−4.4.4 Upon receipt of all the configuration commands, the TM enters the configuration in progress state. The configuration in progress state indicates that the TM is dedicated to the commanded forward and return services demodulator/modulator configuration of the unit. Upon completion of initializing all applicable circuits to the configuration, the TM transitions to the configured state. This state indicates that the TM is ready to accept the Start PN Model command and Start Acquisition command. The Start PN Model command supplies forward PN epoch time for spread modes. Start of this command resets all forward control commands in the PN model (such as Doppler control, etc.).

4−4.4.5 Upon receipt of a Start Acquisition command, the TM attempts to acquire the signal (demodulator section) as previously configured. Any reconfiguration command during this state transitions the TM to the configuration in progress state. Upon receipt of a carrier/phase lock status, the TM transitions to the track and in service state. This state indicates that the TM is providing the configured modulated signal, has achieved lock, and is tracking the signal. This is the only state that the tracking report data is valid. The TM stays in this state until a command requiring a state change is received. (A loss-of-lock situation does not revert the TM to the acquisition state.)

4−4.4.6 During the configured, acquisition, and track and in service states, the TM allows for other commands to be accepted: Start FWD BER Test command, Start RTN BER Test command, and Measure Time Interval command. The Start FWD BER Test command sets up and initiates BER testing of the forward channel via the CMD BERT test set. The Start RTN BER Test command sets up and initiates BER testing of the return I and/or Q channels via the PTE I and Q BERTs. In response to these commands, the TM sets up the CMD, I, and Q BERTs for a mode test with BER options selected. This command specifies the test interval (number of bit cycles for each BER measurement) and the test period, which specifies the total test time (normally the service time) of the test to be performed. Test measurements and elapsed time continue during an out-of-sync condition, which is reported as status. Resync is automatically performed by the CMD BERT. The CMD BERT runs the test for the test period specified, and updates its status upon completion of each test interval. Once a BERT test is started, it may be restarted/stopped in the middle of a test by resending this command, with a new set of start/stop parameters.

4−4.4.7 The Measure Time Interval command sets up and initiates time interval testing for return channel data delay of the return I and/or Q channels via the HP 5316B Universal Counter (TIC). Upon receipt of this command, the TM sets up the TIC for the time interval A to B mode, positive slope trigger. In this mode, the TIC is set up to make a one shot measurement of the delay between the pattern sync transmit pulse and the pattern sync receive pulse of the associated BERTs (I or Q channel BERTs). These sync pulses in the BERTs are square waves which alternate once during each pattern cycle. For the receive pulse to be valid, this measurement must be made only when the BERTs indicate pattern sync. This command provides the counter with the detection voltage trigger level, approximately at the center of the peak-to-peak sync pulse levels.

4 - 5 Forward Service Simulation

4 - 5.1 Introduction

4−5.1.1 The PTE (the TM and associated test equipment) receives and processes forward data signals to support forward link verification testing (for the Modulator/Doppler Predictor). The PTE generates and provides baseband data and clock outputs to the control HWCI. The control HWCI supplies the forward link generation equipment with this test data. The PTE simultaneously receives and processes the USS forward signals with signal parameters and constraints as configured by the control HWCI. The TM applies Doppler pre-correction and follows a commanded profile (ephemeris data), instantaneous frequency at half-second intervals with linear interpolation between points. The time between updates of the profile is two milliseconds, maximum, for all supported modes. The TM processing includes signal acquisition, data recovery, tracking,

coherent carrier and PN reference for return link signal generation (EET only), and forward (baseband) data and clock generation (command channel data and clock). During acquisition, the process is different for pre-service testing (this mode intentionally synchronizes and follows the MDP's frequency sweep for faster acquisition) than it is for the EET state.

4−5.1.2 PN and Carrier pre-service acquisition are parallel events and their acquisition start times are coincident with the Start Acquisition command. Acquisition time includes the time to acquire the PN code (spread modes) and the carrier. Acquisition time does not exceed one second for SSAF, KSAF, SSHF, and MAF services for the specified C/No values and the input signal dynamics are within +/-100 Hz and +/-1 Hz/second. PN and Carrier end-to-end acquisition are parallel events and their acquisition start times are coincident with the Start Acquisition command and the forward service signal being present. Acquisition time includes the time to acquire the PN code (spread modes) and the carrier. Acquisition time does not exceed five seconds for the command channel and 10 seconds for the range channel for SSAF, KSAF, and MAF services, and 20 second for SSHF for the specified C/No values and the input signal dynamics are within +/-100 Hz and +/-1 Hz/second.

4 - 5.2 Demodulator Carrier Acquisition and Tracking

4−5.2.1 The TM incorporates a single-channel demodulator structure to provide the necessary tracking performance for all SSA and MA return test modes and all supported KSA test modes. The single-channel demodulator architecture is shown in figure 4-5.

4−5.2.2 The demodulator consists of a single-channel carrier tracking loop to demodulate the quadrature (Q) signal components. The received Q waveform sets are despread by multiplication with the appropriate Q channel reference code prior to the integrate-and-dump (I/D) filters. For nonspread modes, the code reference is set to all one's. In addition, the reference code pulse shape matches the channel symbol type (NRZ or biphase). Through biphase half-symbol inversion, biphase symbol formats are effectively removed prior to the matched filters, simplifying carrier and PN loop operation.

4−5.2.3 The received Q channel components are processed with the I_Q and Q_Q I/D filters matched to the Q data symbol rate. The carrier loop receives timing information for the I/D filters from its corresponding integrated symbol synchronizer loop. The carrier loop independently computes and filters its phase error measurement, where the phase measurement is made using a decision-directed phase detector. The demodulator then weights the I and Q channel-accumulated phase error terms relative to the symbol rates and power imbalance and sums the two weighted error terms to create a final error term into the loop filter. This minimizes the magnitude of the resultant crosstalk terms and maximizes the signal-to-noise ratio into the carrier loop filter.

4−5.2.4 The phase measurement weighting, final phase error generation, and the loop filtering functions are performed in the firmware. This provides ease of bandwidth change as the data rate varies and allows variation in the filter order between acquisition and track modes. The loop filter output is then applied to a numerically controlled oscillator (NCO), which subsequently controls the phase of a digital phase rotator. The loop filter and NCO control are updated at the lower channel symbol rate, in general, with a minimum sampling rate on the order of 800 sps.

4−5.2.5 A key feature of the carrier acquisition process is the use of a flexible discrete FFT element within the carrier phase detector. This FFT provides fast-acquisition capabilities while eliminating carrier false lock concerns. The FFT operates coherently over the frequency estimation period to provide excellent frequency error estimation capabilities even with minimum carrier-to-noise ratio (C/No) conditions. With frequency acquisition performed primarily by the FFT, the carrier loop needs only to perform simple lock-in, resulting in fast and predictable acquisition performance. During acquisition, the carrier loop operates as a first-order loop to provide fast lock-in while minimizing transient effects. Once acquisition is detected, the loop switches to a third-order loop structure to provide excellent tracking capability even for worst-case dynamics.

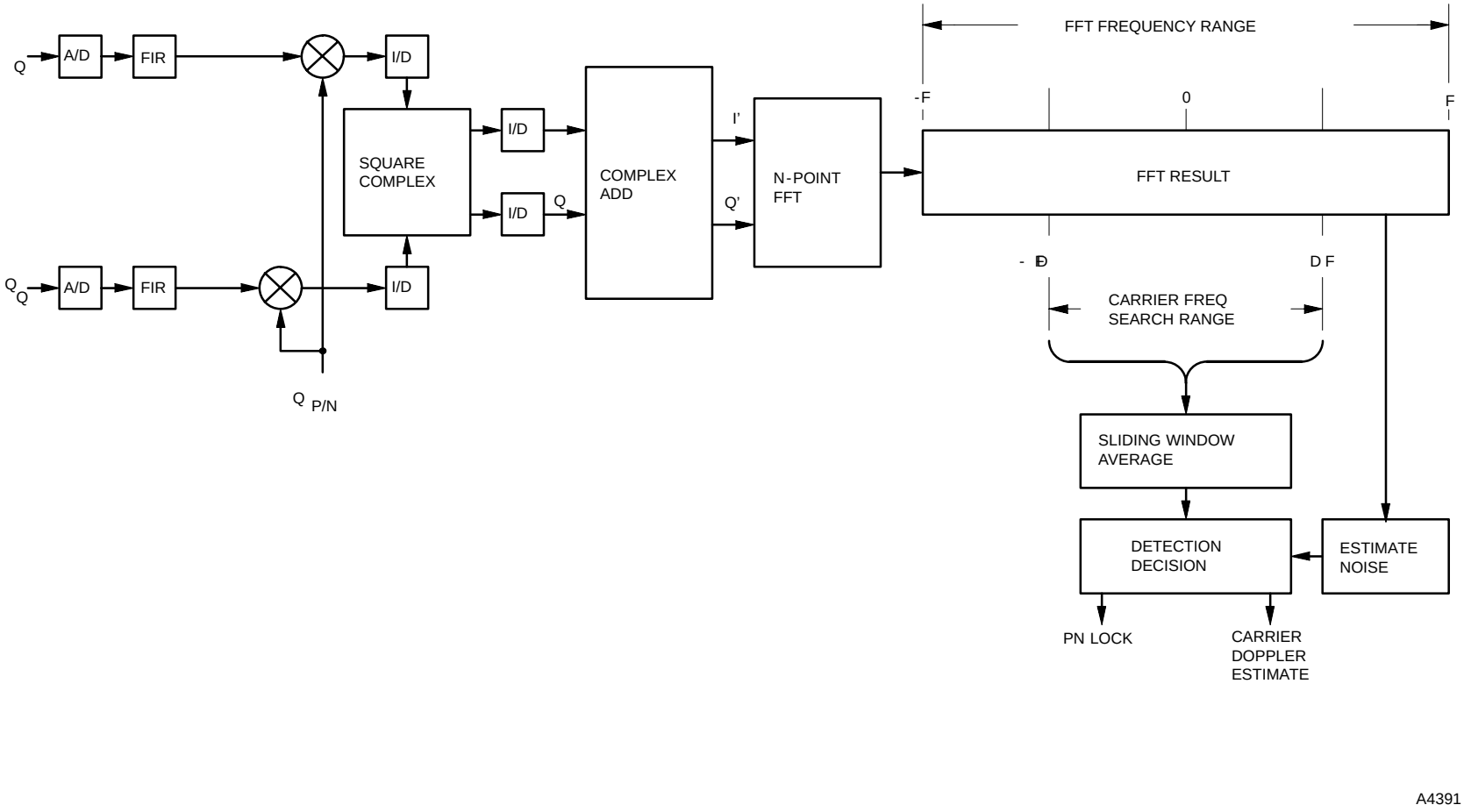


Figure 4 - 5. Carrier Acquisition Functional Block Diagram

4 - 5.3 Demodulator PN Acquisition and Tracking

4−5.3.1 To achieve PN acquisition at all data rates within one second or less for a C/No of 36 dB-Hz, the TM utilizes two 4-to-1024 tap 2-bit correlators operating in parallel. This provides the necessary acquisition capability under all conditions, even with Manchester coding at 1000 sps in DG-1 mode 3, which is the most difficult acquisition mode. A 1024 FFT is included in the process to provide a significant speed/performance improvement through the use of parallel Doppler bin processing. Correlation is performed using two bits only from the I/Q FIR signals with the TM generated replica codes. The replica codes are controlled by MCP and generated by PNP.

4−5.3.2 The code correlation process takes place in the DMSS with its outputs (Q acquisition signals) being input to the MCP-controlled ACQR. ACQR is configured for coherent and non-coherent correlator combines. Coherent combining is used to increase the correlator gain and reduce random noise whereas non-coherent combining is used to increase the gain at the magnitude detector output. Dwell timing/correlator taps are configured as per the dwell period to be used. The dwell period is based on the code uncertainty, symbol format, symbol rate, and PN chip rate. The code uncertainty is based on the ephemeris data. Once the dwell period is determined, the PNP cascade counters are set (T'coh, Tcoh, Td', and Td).

4−5.3.3 During PN acquisition, the MCP controls the search over the range of code and Doppler uncertainty and provides code offsets and Doppler estimates to the DMDP. The search interval function is performed by updating the PN code state and NCOs to search the code and Doppler uncertainty based upon the mode. Next, code offset is computed by determining a code offset calculation every peak detect interrupt event. PN acquisition does not transition to PN tracking until carrier frequency acquisition occurs. For the DMDP to verify the presence of a carrier signal, the signal must be despread and supplied the starting carrier Doppler frequency for the DMDP's search interval (for spread modes only).

4−5.3.4 The despreading is done by using the calculated code offset to update the TRK PN code generator. The code Doppler value that was used at the start of this search interval is used to set the frequency of the TRK code NCO. The corresponding carrier Doppler value is passed on to the DMDP. This initiates the DMDP to do an FFT search over the search interval (see figure 4-5). Once carrier frequency acquisition has been achieved, PN acquisition transitions to PN track.

4−5.3.5 PN tracking is performed using a coherent delay-lock loop PN tracking process (see figure 4-6). Once in the tracking mode, the code loop is aided with the DMDP's measured carrier Doppler, TDRS Doppler, and receive compensation values. The TRK code NCO is updated every 10 milliseconds using a second-order tracking loop with the loop coefficients supporting a 0.5-Hz loop bandwidth to provide good noise characteristics and to minimize peak bias errors during high dynamics conditions.

4 - 5.4 Demodulator Symbol Synchronization

4−5.4.1 The TM utilizes a single symbol synchronizer for the Q data channel. The synchronizer loop, realized almost entirely with digital hardware, is a flexible structure easily adjusted to match received symbol format, anticipated symbol energy to noise ratio (Es/No), and symbol jitter through phase detector reconfiguration and TM control of the synchronizer loop bandwidth.

4−5.4.2 The decision-directed symbol synchronizer is inherently capable of providing the required synchronization capabilities for both NRZ and biphase symbol formats. This synchronizer is decision-directed in that the polarity of the timing estimate out of the timing I/D process is dependent upon the polarity of the data decision. For a symbol synchronizer, timing information is available given only that there was in fact a data transition. The decision-directed synchronizer continually monitors for transitions and updates the loop only when one is detected. This approach provides optimum performance even as the transition density decreases or long periods of no transitions are encountered.

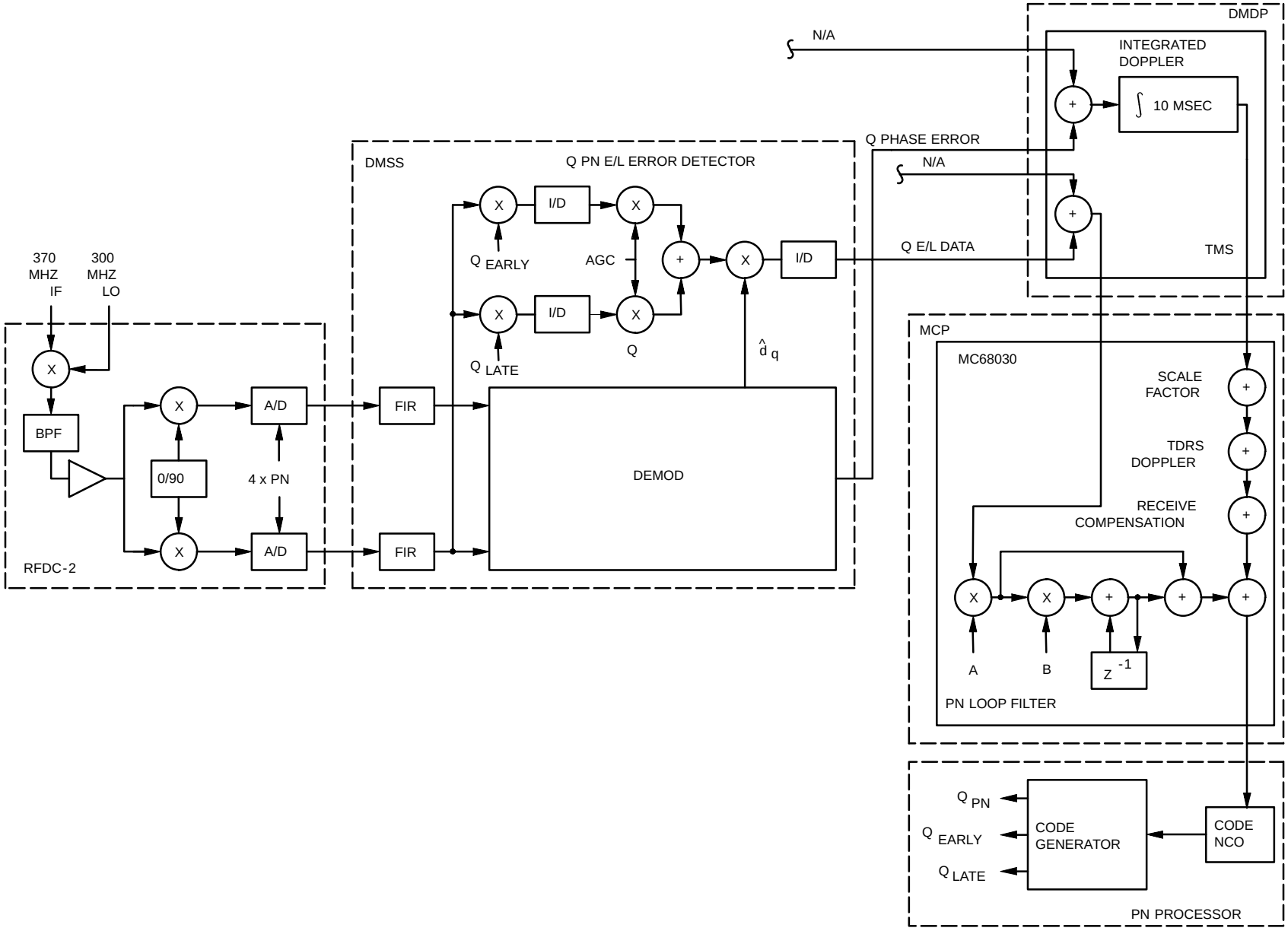


Figure 4 - 6. PN Tracking Functional Diagram

4−5.4.3 The symbol timing phase-error detector is optimally reconfigured to match the received symbol format, either NRZ or biphase. The loop filter bandwidth is varied to best match the anticipated received symbol jitter and Es/No. For biphase symbols, the synchronizer performs integrations every half bit, the first centered over the first transition with the second around the middle transition. The decision-directed synchronizer takes advantage of derived knowledge of the biphase waveform to provide excellent tracking characteristics with biphase data. Since there is always a mid-symbol transition with biphase symbols, the mid-symbol I/D result is always applied to the loop. The start of symbol integration is applied only when a transition is detected, per the case of NRZ symbols.

4−5.4.4 For NRZ symbols during acquisition, the synchronizer integrates over a full window to cover the full timing uncertainty. During tracking, however, the synchronizer narrows the timing integration window down to provide superior noise performance/tracking capability. This benefit is achieved given the dual set of integrations required to optimally synchronize to biphase symbols.

4−5.4.5 The timing loop filter drives a direct-sine NCO that functions as the primary clock source for the channel. This provides continuous timing adjustment capabilities for all modes. The NCO output is converted up to a 12-MHz to 24-MHz frequency range to allow generation of all channel-dependent clocks from this one source. For DG-2 and Shuttle modes, the upconverted NCO output is applied directly to the appropriate input ADCs as the sample clock, and are divided down to create all necessary symbol rate clocks. For DG-1 modes, the A/D output is sampled relative to the PN code rate although all symbol rate-dependent sample clocks are derived in accordance with DG-2 modes.

4 - 5.5 Demodulator AGC

4−5.5.1 The TM provides an independent data AGC loop with control to provide consistent soft-decision levels for the Q data channel. A noncoherent AGC approach, where the AGC attempts to maintain a constant signal-plus-noise level for the analog input signal going to the ADCs, provides for relatively simple implementation with good performance characteristics. The coherent AGC adjusts and maintains a constant signal level to the decoder and carrier loop functions to optimize their performance.

4−5.5.2 As shown in figure 4-7, digital scaling is employed to guarantee uniform performance of all loops. Being digital in nature, the gain in all applicable processing paths (carrier, symbol synchronizer, and PN tracking loops) is identical. The Viterbi decoding algorithm is relatively insensitive to gain variation or equivalently, soft-decision threshold errors. Thus, operation over a relatively wide dynamic range is possible with a non-coherent AGC with minor impact to BER performance. The AGC's operating point is optimized for 10^{-5} decoded BER performance. A first-order AGC loop is implemented with a bandwidth less than 1-Hz to minimize its effect on carrier and PN tracking loops. This bandwidth is sufficient to allow good tracking during worst case specified fade conditions.

4 - 5.6 Ephemeris Processing

4−5.6.1 Ephemeris processing maintains an ephemeris database with a maximum size of 50 minutes worth of data. The TM is capable of saving ephemeris updates up to 60 minutes past its current time. Any ephemeris data greater than 60 minutes in the future is discarded. Ephemeris data provides for precorrection of the carrier and code (see figure 4-8). Demodulator range, Doppler, and time transfer measurements are all made as a byproduct of the implementation of the carrier and code tracking loops in the TM. The tracking loops operate in the closed-loop fashion of error detection, filtering the error, and using those to generate a replica of the input signal, which is beat against the input, and so on. Clearly, if the loop is perfectly locked to the input, then the replica has the same frequency and phase characteristics as the input.

4−5.6.2 In the TM there are two loops, a code tracking loop inside the carrier tracking loop. After lock is achieved, the error signals represent carrier and code phase offset and are generated from the carrier phase detector and PN early/late detector. The carrier and code loop NCOs are used as the primary point of control after the process is initialized by setting the code generator phase and zeroing of the NCO accumulators. NCO updates

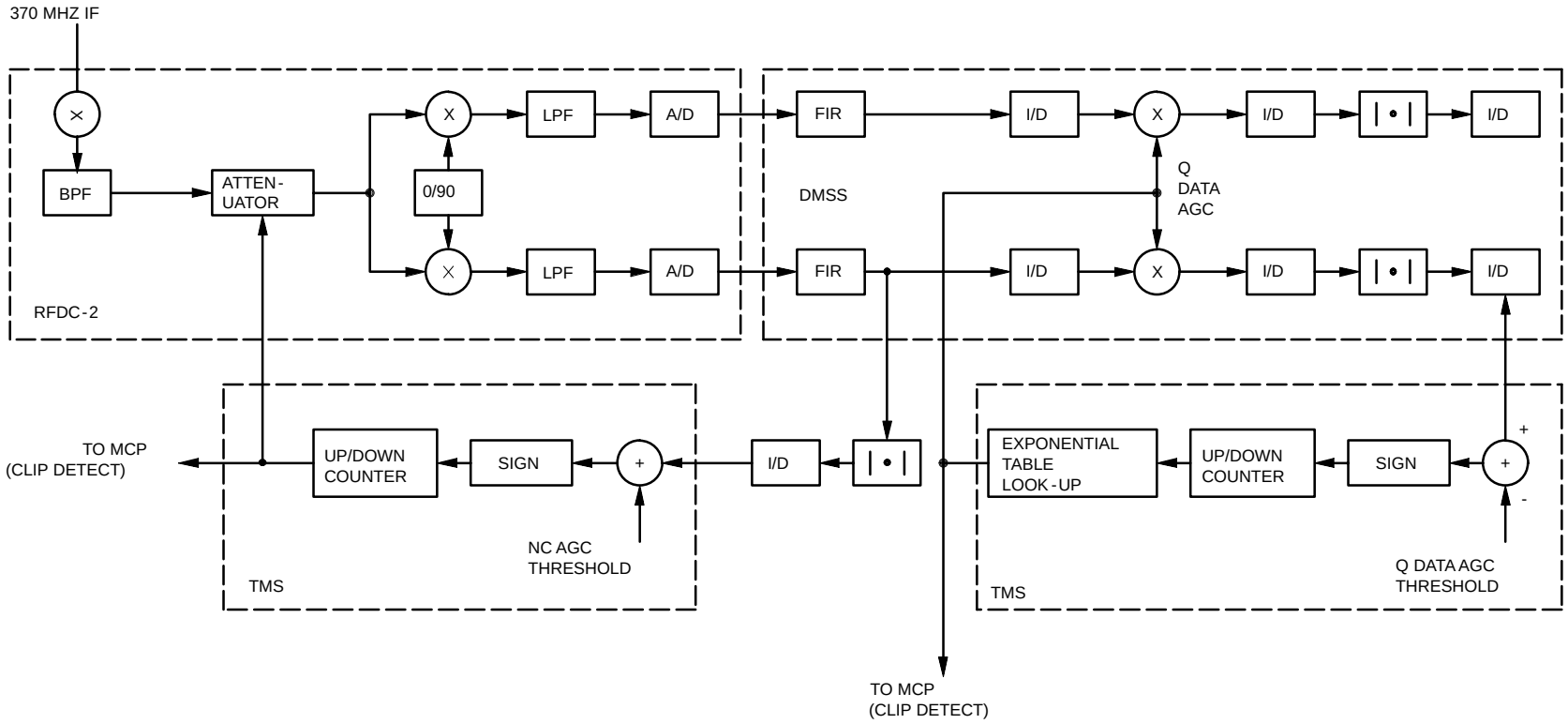


Figure 4 - 7. Coherent/Non-Coherent AGC

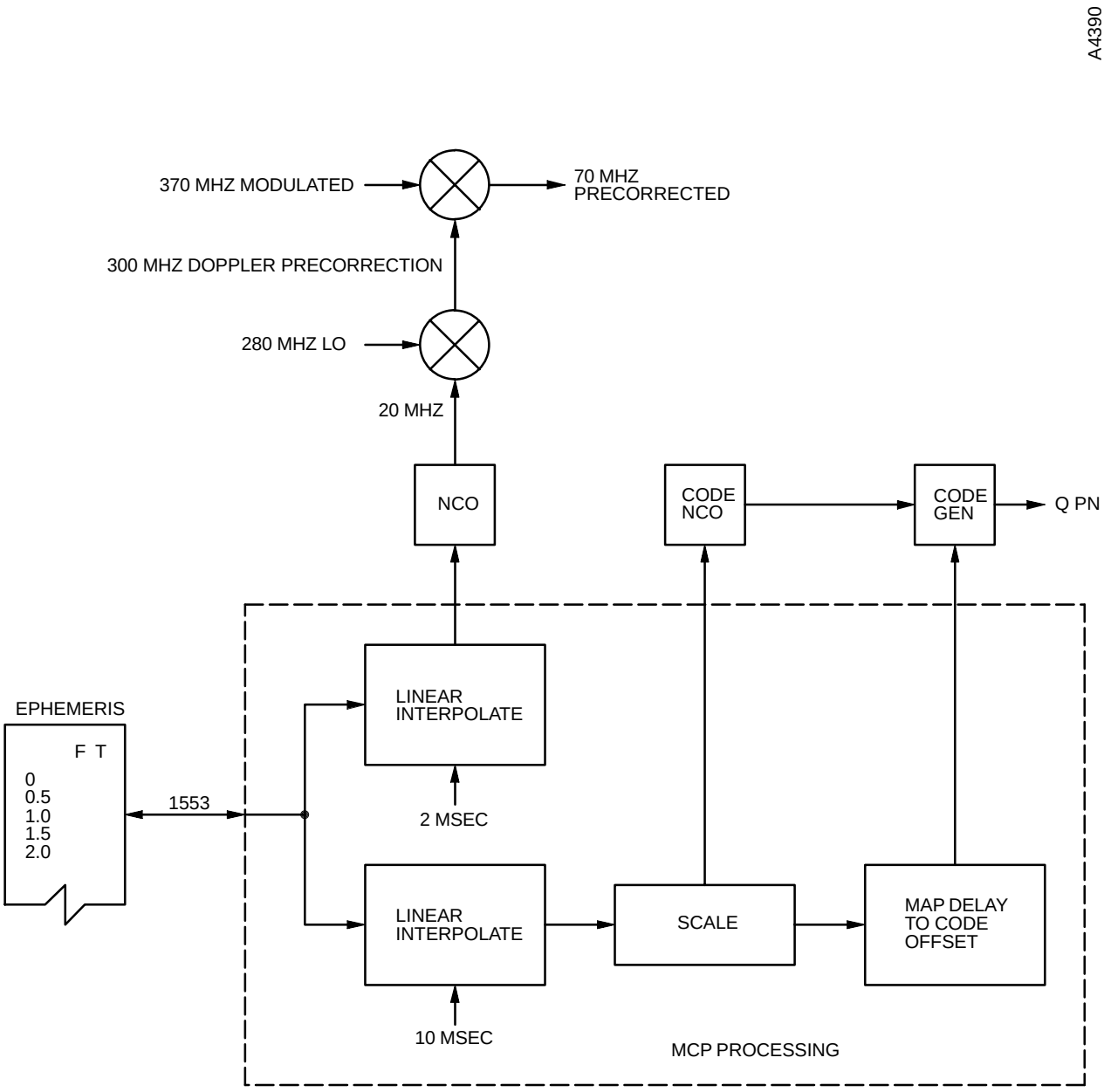


Figure 4 - 8. Ephemeris Precorrection Functional Diagram

are loaded into the control register nominally at a 1-kHz rate for the code loop and between an 800-Hz and 20-kHz rate (variable as a function of data rate) for the carrier loop. The system strobe is synthesized from the precision 10-MHz input, thereby ensuring that the period over which a control word controls the NCO is precisely known. The NCO control word actually represents phase rate. Since the maximum count of the accumulator represents one cycle out of the NCO, the control word is scaled as the phase changes over each update period of the update strobe, with the resolution of each update controlled by the size of the accumulator. The TM uses 24-bit accumulator NCOs, resulting in a phase update as small as 0.3745 microradians per update clock. The update strobe must be at least twice as fast as the highest Doppler offset the loop is required to track.

4−5.6.3 The TM is designed to cover the entire S-band range using only the NCO in the carrier tracking loop, since the input “coarse NCO” which does the down conversion from 370 MHz to 70 MHz is used to make Doppler correction only for K-band service. (This is also driven by the MA service, since the coarse NCO is not in the MA signal path.) The maximum S-band Doppler, assuming 15 km/sec velocity, is 115 kHz. Over a system strobe period, the NCO phase may then change as little as 4.49 microradians, or as much as 115 cycles. This is important because due to the precision intervals over which the control words and strobes operate, it is sufficient to know what control words were applied to the NCO to know precisely the output of the NCO and the internal phase of the NCO. Since the NCO output is the replica of the input signal, the TM knows the characteristics of the input signal automatically as a byproduct of locking to the carrier and PN code, functions that are required even if no tracking services were required (TM requires no tracking services but has the capability as specified above).

4−5.6.4 The noise performance of the loops is a function of the averaging interval, the loop bandwidth, the C/No into the loop, and the noise characteristics of the loop types. Based upon a 1-second average period, the TM generates range and time transfer measurements with a standard deviation of only two nanoseconds at a very conservative worst-case C/No of 26.9 dB-Hz. In addition, specified range-rate measurement accuracy is met for all symbol rates under simulated free flight and powered flight dynamics.

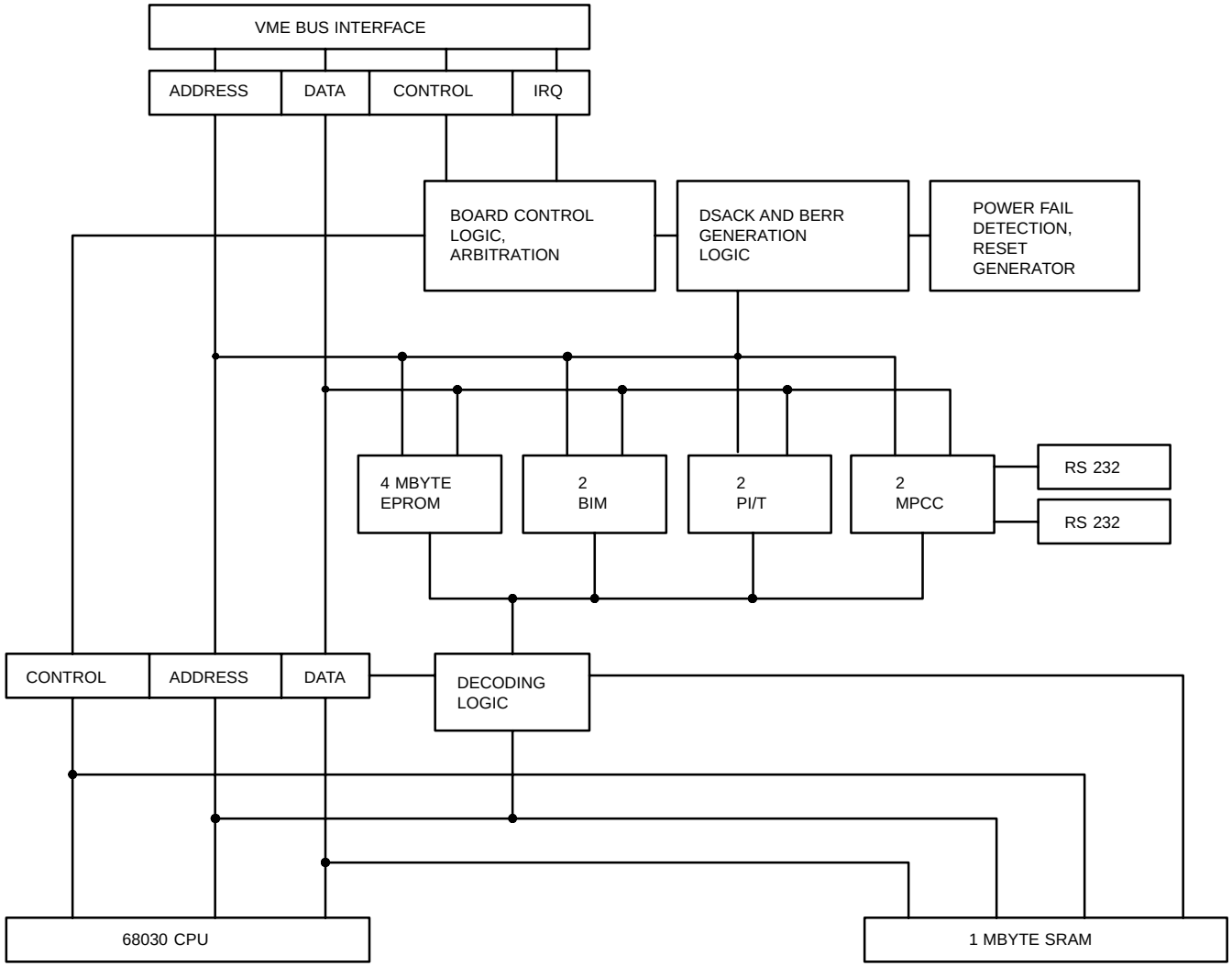
4 - 6 Return Service Simulation

4−6.1 The TM and associated equipment (PTE) provide all test signal modulation functions and all recovered baseband data processing necessary to support all KSA, SSA, and MA return service verification/testing of the Integrated Receiver. The PTE automatically calibrates and generates return IF test signals plus additive white Gaussian noise (AWGN) ranging from a C/No of 27 dB-Hz to 88 dB-Hz as commanded by the control HWCI. The PTE generates return test signals and provides error detection capabilities on the recovered baseband I and Q data with the signal parameters and constraints as configured by the control HWCI.

4−6.2 The PTE generates independent I and Q data channels at rates commanded by the control HWCI. Clock frequencies are variable from 100 Hz to 6 MHz for the Q channel and from 100 Hz to 12 MHz for the I channel. The data signals on the I and Q channels can be independent and asynchronous. For independent I and Q channel data signals, the sum of the data rates on the I and Q channel can not exceed the total maximum rate as specified. When biphase format conversion is commanded, the maximum data rates are reduced by a factor of two. For DG-2, the maximum data rates are reduced by a factor of two for rate 1/2 coding and by a factor of four when both rate 1/2 coding and biphase conversion are used. The maximum data rates are reduced by a factor of three for rate 1/3 coding and are reduced by a factor of six when both rate 1/3 coding and biphase conversion are used.

4 - 7 Modem Control Processor

Refer to figure 4-9 for the following MCP functional description. MCP consists of a 25-MHz 68030 processor based VME bus controller 1-Mbyte zero-wait state static RAM, four EPROM sockets (27C010 EPROMs = 512 kbytes), 32-bit VSB master interface, two serial channels (68561 based) - up to 38.4 kbaud (RS-232 compatible,



A4253

Figure 4 - 9. MCP Functional Block Diagram

one channel selectable RS-232/RS-422/RS-485), and two 24-bit timers. The MCP address select enables the control logic section of the slave boards on the VMEbus by matching address lines A23-A19 with the board select bits of the P2 connector. The remaining 18 address lines (A18-A01) are then used by the control logic to determine the transfer function to be processed.

4 - 7.1 68030 Microprocessor

4–7.1.1 The 68030 contains 16 32-bit general-purpose address and data registers, two 32-bit supervisor pointers, and one user stack pointer. The non-multiplexed address and data bus can be used in an asynchronous mode to allow optimized hardware interfacing to the buses. Synchronous bus cycles are also supported by the 68030 to accelerate transfers. To offer high data throughput in conjunction to the static RAM, a 16-MHz CPU clock frequency is provided. The 256-byte on-chip data and instruction caches provide a maximum computing rate of 8 MIPS by unloading the system buses from opcode/program fetches.

4–7.1.2 The data bus interface of the 68030 is very flexible and provides a dynamic bus sizing where the data bus size can be adapted. This feature allows the interfacing of 8-, 16-, or 32-bit organized memory and/or I/O devices. For easy exception handling and recover of bus errors, the 68030 stores all internal states in the stack. The MCP contains a local bus interface (LBI). The following devices are connected to the LBI: local SRAM, EPROM, serial I/O controllers (2), parallel interface and timers chips (2), and local interrupt handler chips (2).

4 - 7.2 EPROM/SRAM

The first two read cycles after a reset of the 68030 processor are fetches of the initial interrupt stack pointer and the initial program counter. These cycles are executed under addresses $0 and $4, respectively. A special control logic maps the EPROM down to this address to start the CPU out of the installed EPROMs. The EPROM area is 32 bits wide, offering maximum throughput for the programs running in the EPROMs (SP7472500-XXX). The local SRAM has a memory capacity of 1-Mbyte. The memory module used allows zero wait-state access at the 16-MHz processor clock frequency. The memory is organized 32 bits wide and supports all access modes of the 68030.

4 - 7.3 Serial I/O Interfaces

The MCP contains two RS-232 serial I/O interfaces built around the multiprotocol communications controller (MPCC). The serial interfaces are connected to two 9-pin D-sub connectors on the front panel. One of the two serial interfaces can be reconfigured for RS-422/RS-485 compatibility. Each MPCC interfaces a single serial communication channel using synchronous or asynchronous protocol. In addition to data transfer between the CPU and MPCC, control and status are provided through the 22 directly addressable registers. The on-chip oscillator drives the internal baud rate generator which with two selectable prescalers and a 16-bit divider provides baud rates from 110 to 38400 baud.

4 - 7.4 MPCC Interrupt Handling

Two bus interrupter modules (BIMs) are used to handle all local interrupts. Each MPCC is able to force an interrupt on three different conditions: receiver contains a character, the hardware interface has detected an interrupt generation state, or transmitter is empty. The three different groups of interrupt generation are under software control through some of the 22 registers of the MPCC. The BIM provides a flexible interrupt structure because the interrupt level and the interrupt vector are software-programmable. This allows the adaptation of the RS-232 interface on the main board to a wide variety of applications. The two parallel interface and timer (PI/T) devices are used for local control. One port is assigned for interrupt level control and one other port is used for reading the rotary switches on the MCP. The rotary switches can be used as a general-purpose input channel for diagnostics, configuration selection, or automatic system boot with different configurations.

4 - 7.5 VMEbus Interface

MCP VMEbus supports 8-, 16-, 32-bit, and unaligned data transfers. The extended, standard, and short I/O address modifier codes are implemented to interface to all existing VMEbus products. Each of the seven interrupt request signals

can be connected to the implemented interrupt handler. A single-level bus arbiter and the bus arbitration, which has four bus release options, completes the VMEbus interface.

4 - 7.6 MCP Function Switches and LEDs

The MCP contains four function switches and seven LEDs for board function control. The switches and LED functions are as follows:

a. A reset of all onboard I/O devices is enabled if the RESET switch is pushed to the “up” position. RESET is held active until the switch is in the “down” position. In addition, a local timer guarantees a minimum reset time of two to three seconds. Power fail and power up also force a reset (two-three seconds) to start the board if the supply voltage is out of range (below 4.75 volts).

b. The ABORT switch, which provides an interrupt on a software-programmable level, is provided on the board to allow an abort of the current program, to trigger a self-test, or to start a maintenance program. ABORT is activated in the “up” position and deactivated in the “down” position.

c. The CACHE switch enables the 68030 onchip data cache with its 256 bytes when in the “down” position. In the “up” position, the onchip cache is deactivated by hardware, overriding all software settings.

d. The RUN/HALT (R/H) switch enables or disables local operation of the CPU. This switch can be used to debug multiprocessor software packages and to disable a CPU board in an application when a failure has occurred but power can’t be switched off. The processor is in the halt state if the switch is in the “up” position. Normal operation is provided when the switch is in the “down” position.

e. The RUN LED is green if the processor is not in the halt state. It is red during the reset phase, and when the processor is in the halt state.

f. The SRAM LED is always lit yellow when the processor is accessing the local SRAM.

g. The EPROM LED is lit yellow when the processor accesses the EPROM area.

h. The bus request (BR) VME LED is lit yellow when the local processor requests bus mastership on the VMEbus.

i. The bus master (BM) LED is lit when the MCP is the current bus master.

j. The data strobe (DS) VME LED is lit whenever the processor has placed a data strobe on the VMEbus.

k. The DS VSB LED is lit whenever the processor has placed a data strobe on the VSB. Not applicable to TM operations.

l. The rotary switches are 4-bit hexadecimal encoded. They are completely under software control. Normal IR operation is with the switches in the “F” postion.

4 - 7.7 BERR Handling

The MCP contains a timeout counter to detect if an addressed device or memory does not respond with a DSACK to the CPU. The timeout is fixed, set to 70-80 microseconds, allowing slow VMEbus boards to communicate with the CPU.

4 - 8 IEEE-488 Interface Control

4–8.1 Refer to figure 4-10 for the following I488 functional description. The I488 consists of the buffers, drivers, and transceivers for the address, data, status, and control lines used on the VMEbus, plus other logic circuitry that converts internal signals to bus-compatible signals. The address decoder recognizes, when the VMEbus master addresses one of the I488 registers, and generates the appropriate strobe to effect the data transfer. The timing state machine controls the timing of direct memory access (DMA) transfers and accesses to the I488 from the VMEbus. The clock and reset circuitry monitors the VMEbus utility signals to generate the 8-MHz clock used by the talker/listener/controller (TLC) and DMA controller (DMAC) and to detect system reset, power failure, and bus error conditions.

4–8.2 The TLC, a large scale integrated circuit, implements many of the I488 interface functions, either independently or with assistance of, or interpretation by the controlling program. Together with special transceivers, the TLC forms the IEEE-488 bus interface side of I488. The DMAC, a large scale integrated circuit, controls DMA

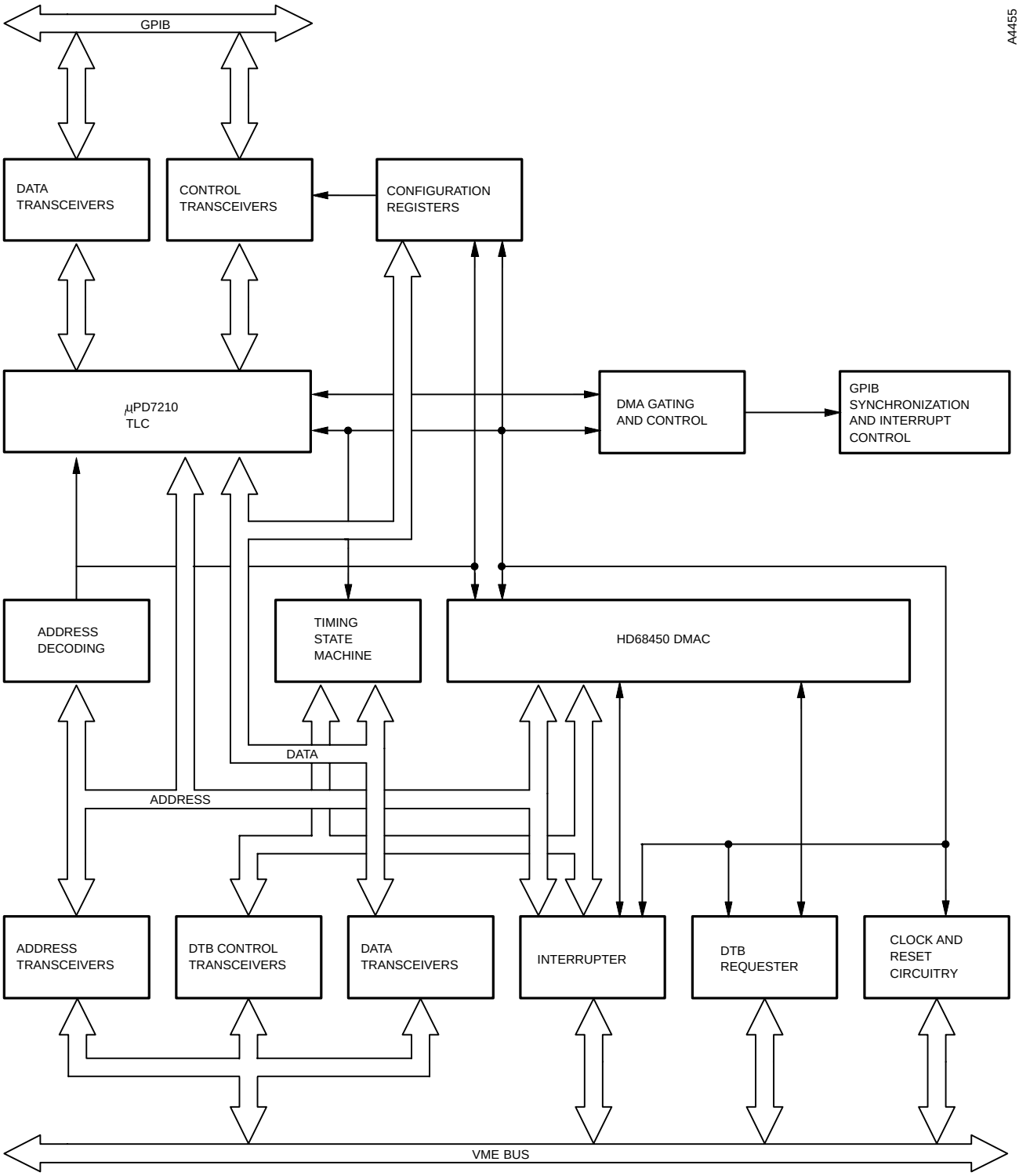


Figure 4 - 10. I488 Functional Block Diagram

transfers between the IEEE-488 bus and VMEbus. The DMA gating and control circuitry controls the DMA request/acknowledge interface between the TLC and the DMAC. The DTB requester performs the necessary VMEbus protocol to request, obtain, and release control of the VME system bus. Once configured for a DMA transfer, the I488 automatically performs data transfers between the IEEE-488 bus and VMEbus memory.

4–8.3 The synchronization and interrupt control detects the synchronization of the I488 after the last byte in a DMA transfer (all devices on the IEEE-488 bus have accepted the last byte) and detects interrupting conditions from the TLC. TLC interrupt requests are routed through the DMAC, which notifies the interrupter when either a TLC interrupt or one of its own internal interrupt conditions is detected. The interrupt implements the proper VMEbus priority interrupt protocol, allowing the I488 to request and respond to an interrupt acknowledge cycle. All interrupt conditions are also detectable by polling.

4 - 9 Timing Generator (1 & 2)

Refer to figure 4-11 for the following TIME functional description. The address select enables the control logic section of the TIME by matching address lines A23-A19 of the VMEbus address with the board select bits of the P2 connector. The remaining 18 address lines (A18-A01) are then used by the control logic to determine the transfer function to be processed.

4 - 9.1 IRIG Decoding

TIME (only TIME1 is used in this capacity within the TM) provides the capability of decoding unmodulated IRIG-B data into components of seconds, minutes, hours, and days, and to buffer these signals to the data lines on the VMEbus when enabled by the control logic. The IRIG-B data is updated and written to RAM between the 0-msec and 500-msec time marks. The data is valid for reading from RAM between the 500-msec and 0-msec time marks. The time components are in binary-coded decimal (BCD) format.

4 - 9.2 1553 Bus Interface

TIME provides a transformer-coupled 1553 bus interface between the VMEbus and the P2 connector. The interface to the P2 connector consists of two transmit/receive transformers and the remote terminal address inputs. The interface to the P1 connector consists of the address and data lines to read/write to 1553 bus control/status registers and RAM.

4 - 9.3 Time Mark Generation

TIME generates 1-, 10-, 100-, 1000-, and 20,000-PPS time marks based on the 50-MHz input in sync with the 1-PPS external signal. The time marks have a duty cycle of 20% and are valid on the falling edge of the pulse. A status indicating the detection of a time synchronization error between the external input 1-PPS and the internally generated 1-PPS signal is provided in the TIME status word. The time synchronization error is set if the 1-PPS external and 1-PPS internal signals differ by more than one 50-MHz clock cycle. A time resynchronization may be commanded through the TIME control register. There is also a flag that is set when the resynchronization process is complete.

4 - 9.4 Interrupt Generation

TIME provides interrupts to the VMEbus consisting of the generated time marks, the 1553 bus interrupt, and the selected epoch interrupt. Any or all of the interrupts can be masked through the interrupt mask register. The interrupts are divided into two separate groups: time interrupts and other interrupts. Each group has a programmable vector in which the upper nibble is determined by the interrupt vector register. The lower nibble is determined by the interrupt generated. The time interrupts interrupt the microprocessor with a level 6 interrupt and the other interrupts with a level 3 interrupt.

4 - 9.5 Epoch Count Generation

TIME provides the time difference between the epoch A or B and the 1-PPS signal with 100-nanosecond resolution when enabled by the control logic. This time difference is valid upon the epoch interrupt of the microprocessor. The difference components are in BCD format. The epoch is

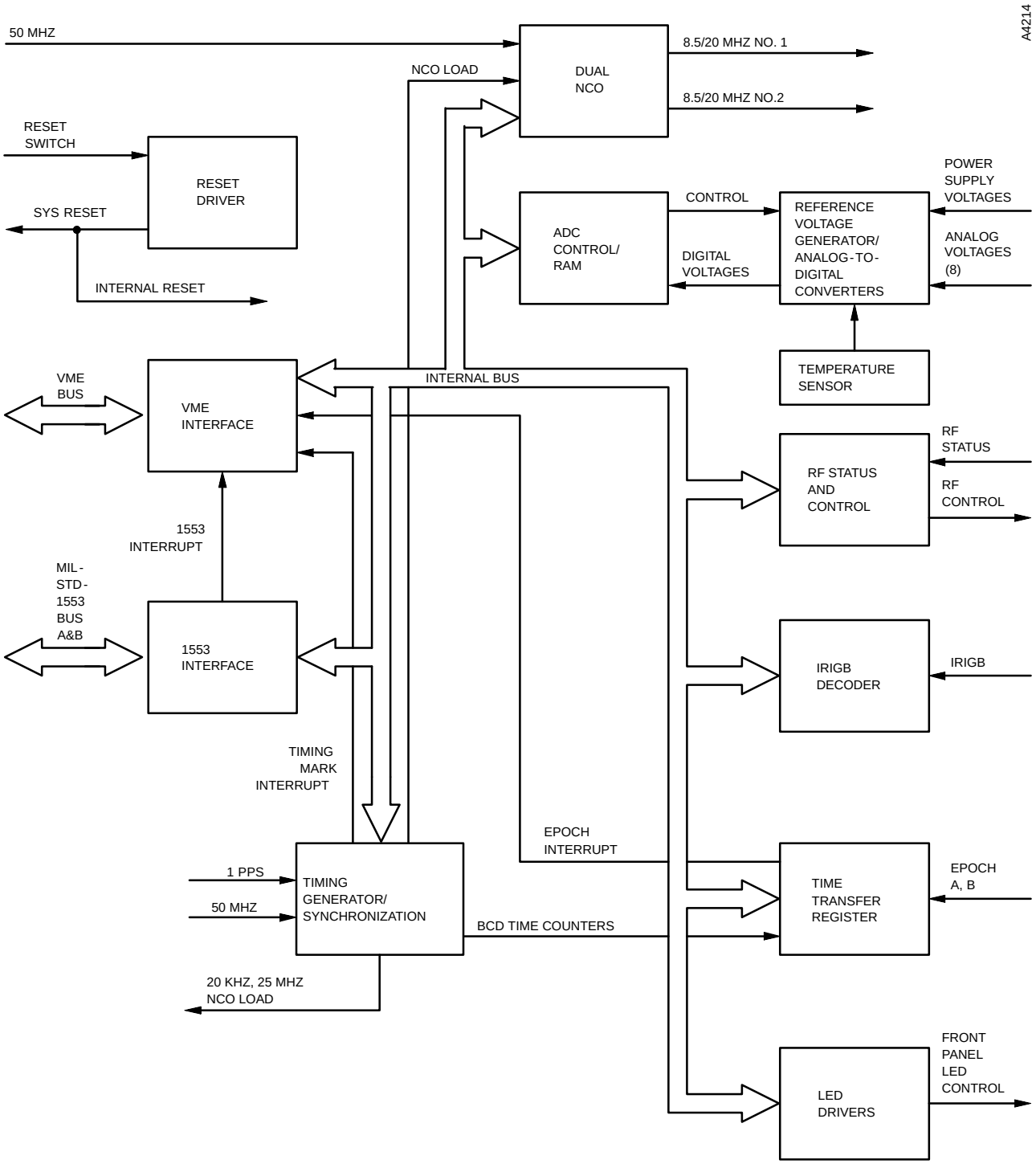


Figure 4 - 11. TIME Functional Block Diagram

selectable between A and B through the TIME control word.

4 - 9.6 NCO Outputs

TIME provides two NCOs that are controlled by the MCP program (via the VMEbus). The NCOs have a sampling frequency of 50 MHz and a 22-MHz lowpass filtered analog output of these NCOs is available through coaxial connectors J1 and J2.

4 - 9.7 Analog-to-Digital Generation

4–9.7.1 TIME provides a digital measurement of various analog voltages to the data lines on the VMEbus when enabled by the control logic. There are 16 possible measurements, and the measurements are updated and written to RAM between the 800-msec and 0-msec time marks; therefore, the measurements are valid for reading from RAM between the 0-msec to 800-msec time marks. Channels 0-7 are predefined and channels 8-15 are user defined. The analog level value register output value is dependent upon the channel being read. The output range is +/- 10 volts, and the LSB is equal to 4.88 millivolts. The output is in offset binary format meaning 0000H = -10 volts, 0800H = 0 volts, and 0FFF = +10 volts.

4–9.7.2 The channels are defined as follows: channel 0 is the -5.2 Vdc and +5 Vdc supply sum, channel 1 is the -12 Vdc and +12 Vdc supply sum, channel 2 is the -15 Vdc and +15 Vdc supply sum, channel 3 is ground, channel 4 is the -6.2 Vdc reference, channel 5 is the +6.2 Vdc reference, channel 6 is the temperature sensor, and channel 7 is the RF 5 Vdc supply. The temperature sensor voltage to degrees C conversion is as follows: 15.0 C = +5.764 volts, 20.0 C = +5.864 volts, 25.0 C = +5.964 volts, 30.0 C = +6.064 volts, etc.

4 - 9.8 Miscellaneous Registers and Control

The TIME test point register provides up to eight test points on the TIME via the P2 connector controllable from the VMEbus. Each point is cleared or set through the corresponding bit in the test point register. The TIME driver register provides eight bits of control adjustable from the VMEbus. This register interfaces to the P2 connector to drive various signals. The TIME also provides the capability of reading a reset switch from the P2 connector and drive SYSRESET* on the P1 connector to reset the unit when this switch is closed for a minimum of 200 msec.

4 - 9.9 RF Status and Control

The RF module provides TTL level RF status signals which provide up to eight bits of RF status information to the VMEbus upon command. Subsequently, eight bits of adjustable control is generated for use by the RF module.

4 - 10 Test Data Interface

Refer to figure 4-12 for the following TDIF functional description. The address select enables the control logic section of the TDIF by matching address lines A23-A19 of the VMEbus address with the board select bits of the P2 connector. The remaining 18 address lines (A18-A01) are then used by the control logic to determine the function to be processed.

4 - 10.1 Clock Interface and Control

The TDIF receives synthesized clocks for I, Q, and command data/symbols. The I and Q clocks are input from the EXCS. The command clock is input from the TIME2. The I clock is variable from 100 Hz to 12 MHz with a resolution of 0.011% (50 MHz/2^{32} = 1.164 millihertz, therefore, 0.011% of 100 Hz). The Q clock is variable from 100 Hz to 6 MHz with a resolution of 0.01% (0.011% for 100 Hz). The command channel is variable form 100 Hz to 25 MHz with a resolution of 0.01% (0.011% for 100 Hz). A doubled command clock is selectable to support clock rates above 21.5 MHz (this is the NCO maximum output frequency).

4 - 10.2 Data Format Conversion

When required for single data DG-2 configurations, alternate bits of a single data stream are demultiplexed onto the I and Q channels. The alternate bit single channel mode puts alternating bits of the I data on the I and Q data channels, as shown in figure 4-13. The TDIF performs data format and conversion on the I and Q data channels independently. The I and/or Q data can be converted from NRZ-L to NRZ-M, S, Biphase-L, M, S data formats as commanded by the MCP. Figure 4-14 is the timing diagram for the data formatting process. Data format conversion

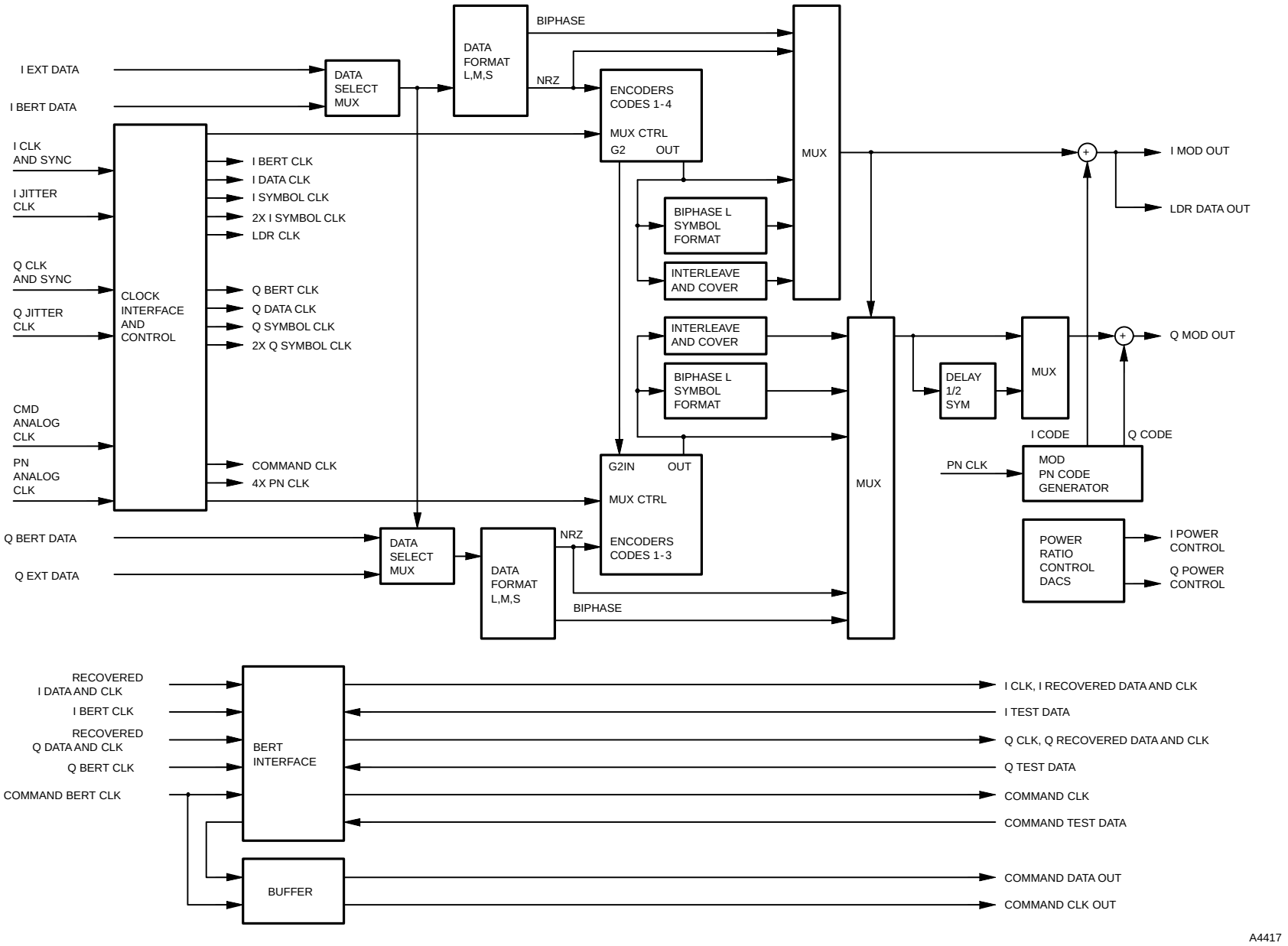


Figure 4 - 12. TDIF Functional Block Diagram

A4411

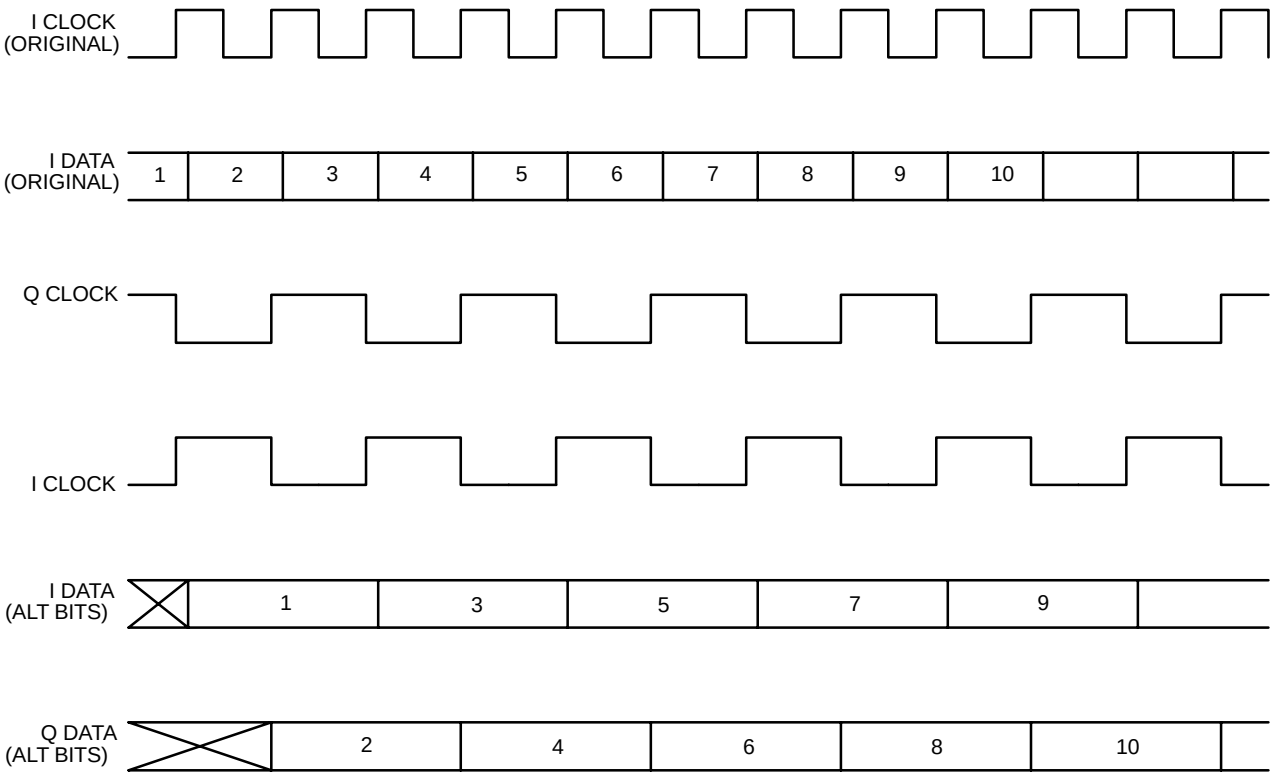


Figure 4 - 13. Single Data Channel Alternate Bits Timing Diagram

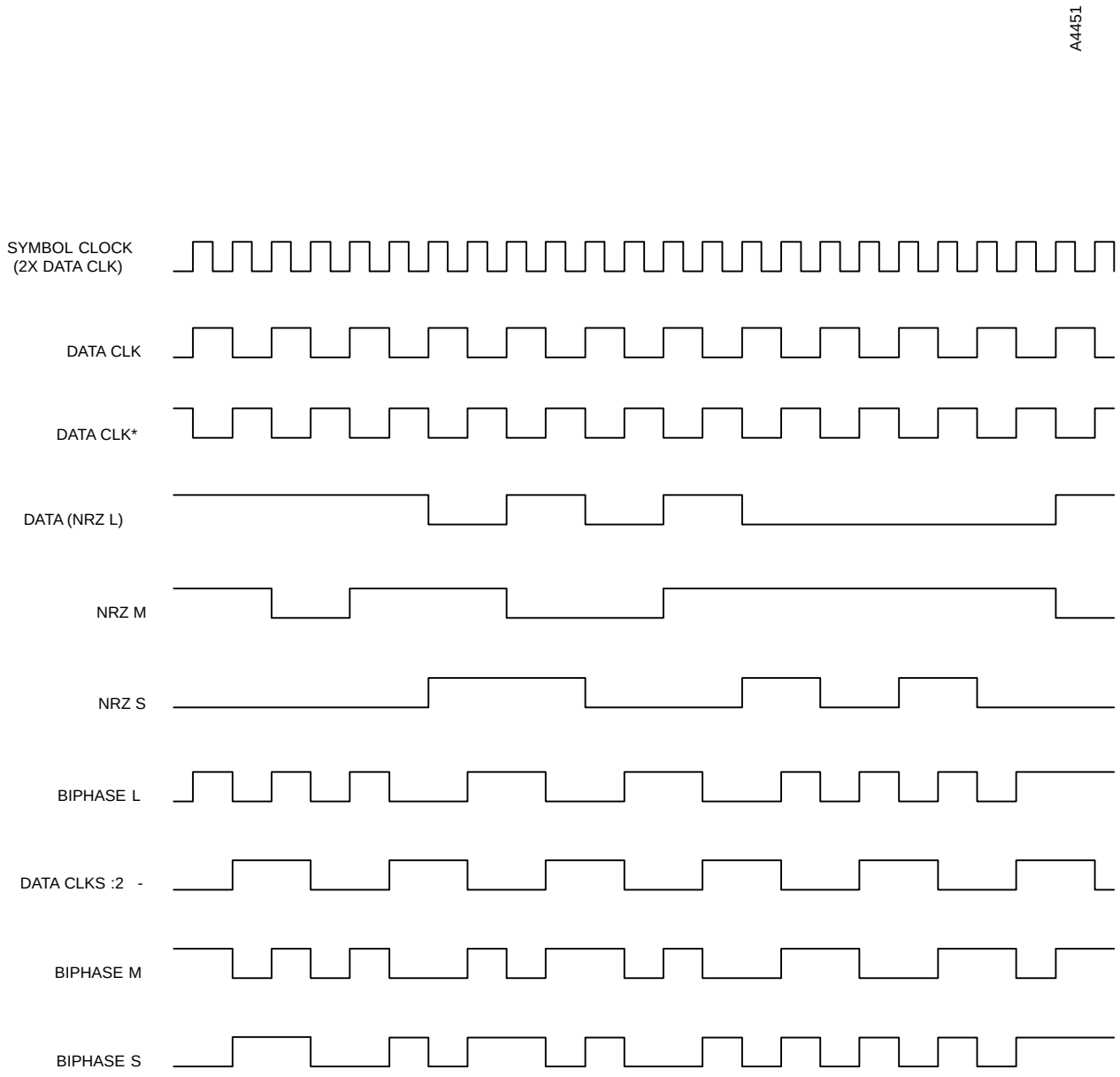


Figure 4 - 14. Data Formatting Timing Diagram

is supported for rates up to and including 6-Mbps. Single data channel demultiplexing is supported for rates up to and including 12 Mbps (I channel only). Data asymmetry is less than +/- 3.0% of a symbol period and data transition time is less than 5.0% of a symbol period.

4 - 10.3 Convolutional Encoding

4–10.3.1 The TDIF supports convolutional encoding for four codes. Code 1 and Code 2 are transparent rate 1/2 codes. Code 3 and Code 4 (Shuttle code) are rate 1/3 with Code 3 transparent and Code 4 non-transparent. Both channels (I and Q) support Codes 1-3 and only the I channel supports Code 4. The generator functions for all four codes are as follows:

Code 1: G1 = 1111001
G2 = 1011011

Code 2: G1 = 1011011
G2 = 1111001

Code 3: G1 = 1111001
G2 = 1011011
G3 = 1110101

Code 4: G1 = 1111001
G2 = 1011011
G3 = 1100101

4–10.3.2 Encoders 1, 2, 3, and 4 are implemented with a single block as shown in figure 4-15. The clocks are equivalent for the I and Q channels. Encoder 1 is realized by multiplexing the output symbols such that the symbol corresponding to G1 precedes the symbol corresponding to G2. The symbol corresponding to G3 is not used for encoder 1. Encoder 2 is realized by multiplexing the output symbols such that symbol corresponding to G2 precedes the symbol corresponding to G1. The symbol corresponding to G3 is not used for encoder 2. Encoder 3 is realized by multiplexing the output symbols such that the symbol corresponding to G1 precedes the symbol corresponding to G2 which precedes the symbol corresponding to G3. Encoder 4 is realized by multiplexing the output symbols such that the symbol corresponding to G1 precedes the symbol corresponding to G2 which precedes the symbol corresponding to Shuttle G3 for Encoder 4. The symbol corresponding to G2 for the I channel encoder 1-3 is made available to the Q channel for single data DG-2 modes (alternate encoder bits go to I and Q data channels). The symbols corresponding to G2 for Code 1 (G1 for Code 2) can be rate 1/3 codes as commanded.

4 - 10.4 Interleaving and Cover Sequence

The interleaver is a (30,116) convolutional interleaver (see figure 4-16). The input symbols are modulo-2 added to a cover sequence. The cover sequence is a 30-bit cyclic binary sequence. The first shift register bit of the initial condition is synchronized with the symbols that result from a zero row address and with the G1 symbol out of the convolutional encoder. The board reset bit in the general control register is used to initiate this synchronization. The I/Q clock input to the TDIF must be running before this reset bit is activated to allow for proper synchronization. The RAM is used to take the place of the shift register and the addresses of the RAM are controlled in a way that will implement the decommutation, variable shift register lengths, and commutation function. Write addresses are controlled by the modulo-30 and modulo-120 counters and the read address is controlled by the modulo-30 counter and the read address PROM. The read address PROM performs the multiply, sum, and modulo-120 functions. The interleaver does a write cycle during the first half of the symbol (while symbol clock is high) and does a read cycle during the second half of the symbol (while symbol clock is low). The interleaver supports symbol rates up to and including 6 MHz.

4 - 10.5 Symbol Format Conversion

The output symbols of the encoder for both I and Q channels can be converted from NRZ to Biphase-L as selected.

4 - 10.6 PN Spreading

The TDIF generates all PN codes necessary to support return PN code generation. These codes include short (DG-1 Mode 2), and long (DG-1 Modes 1 and 3) PN codes. The PN code generator is designed to be identical to the tracking PN code generator on the PNP. The PN codes are generated by using an STEL 1032 PN code generator. The STEL PN code generator normally is used to load the PN RAM but the PN RAM can be loaded over the VMEbus if necessary. The TDIF receives a PN clock (4X PN code rate) from the TIME2

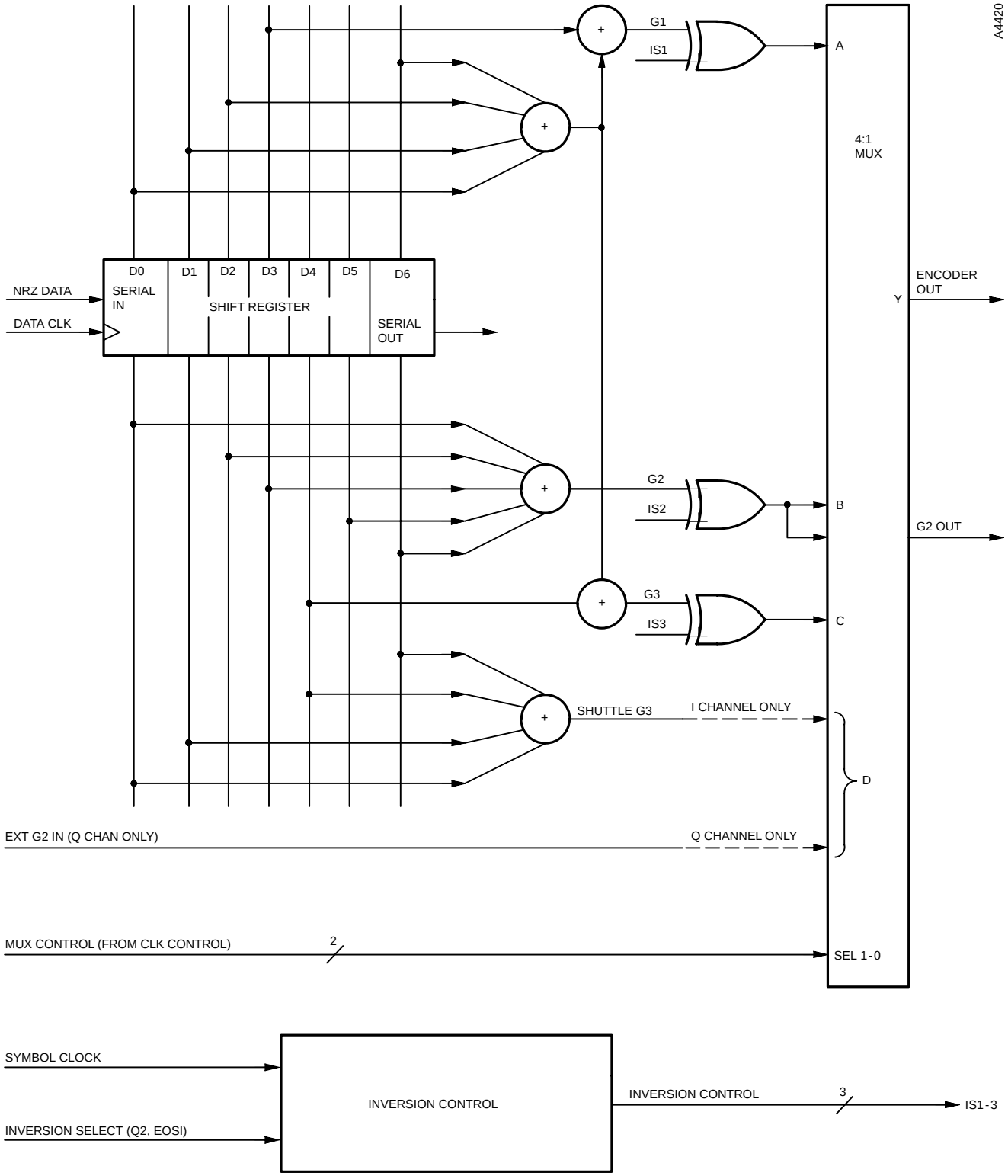


Figure 4 - 15. Convolutional Encoder

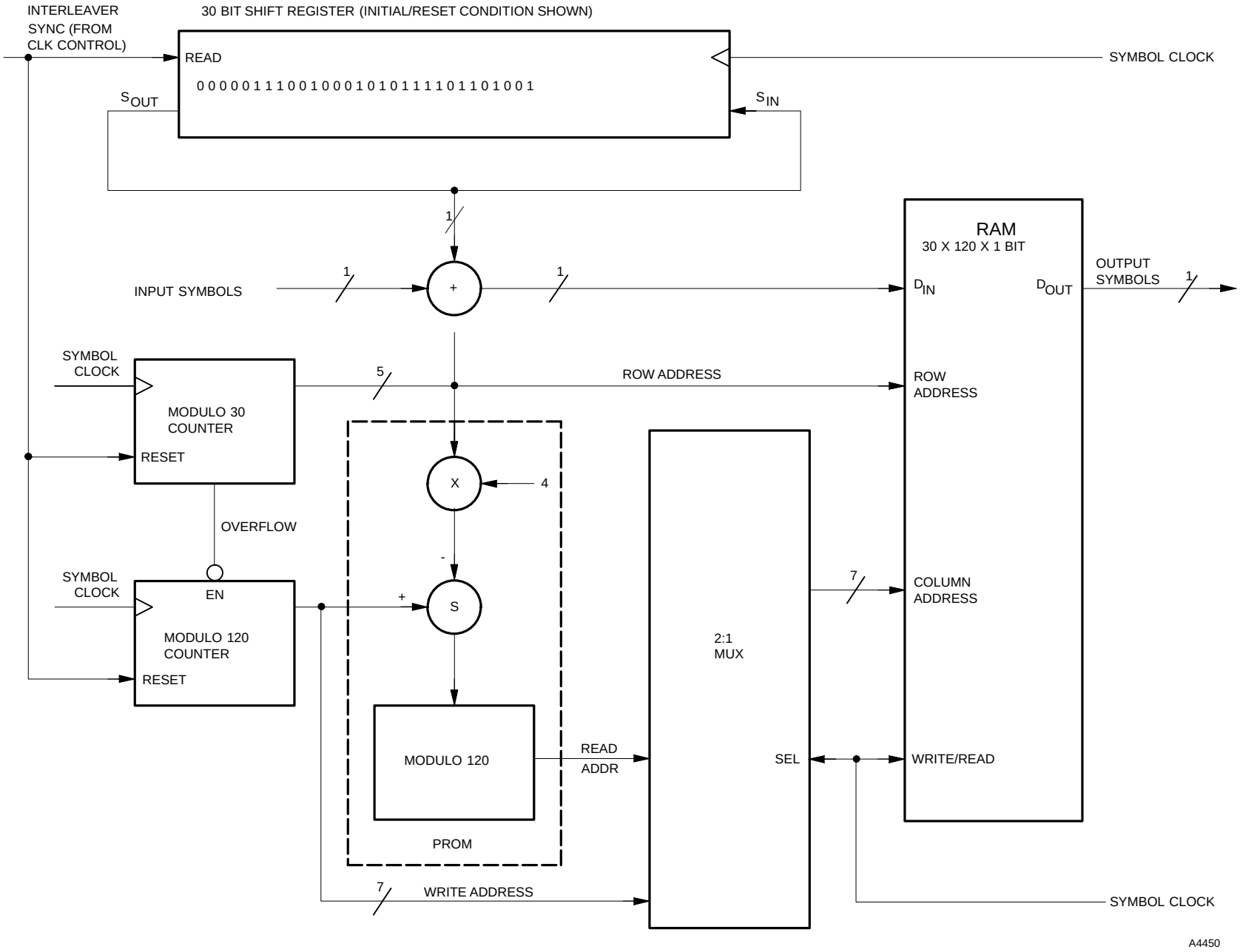


Figure 4 - 16. Interleaver/Cover Funcational Block Diagram

which drives the PN generator. The clock has a nominal frequency of 12 MHz and is capable of supporting Doppler simulation and coherent turnaround. The clock is derived from an NCO and associated logic (on the TIME2). The PN generator supports rates up to and including 4.0 Mcps.

4 - 10.7 External Test Data Inputs

The TDIF receives external data and clock inputs (differential TTL) for I and Q data channels. The I, Q, or both I and Q external test data can be selected as the indicated data source instead of the BERT input test data. The external data is limited to 12 Mbps for the I channel and 6 Mbps for the Q channel.

4 - 10.8 BERT Interface

The TDIF provides all necessary drivers and receivers to interface with the BERTs (I, Q, and CMD). The BERT interface is single ended TTL with 30-ohm line drivers driving the outputs and standard fast TTL inputs terminated in approximately 50 ohms for all inputs. The BERT interface supports the following data rates:

a. I data channel: 100 bps - 12 Mbps.

b. Q data channel: 100 bps - 6 Mbps.

c. Command data channel: 100 bps - 25 Mbps.

4 - 10.9 VMEbus Interface

The TDIF has a VME interface in order to support interfacing with the MCP. The TDIF operates under control of the MCP and provides status to the MCP as necessary to support return service test signal generation. The interface is through various control and status registers. All bit definitions have bit 15 as the MSB and bit 0 as the LSB.

4 - 10.10 TDIF Registers

4–10.10.1 The general control register controls the TDIF functions not specific to a particular channel. The address offset of the general control register is 10008 (word access). The I channel control register is used to control data formats, select encoders, select interleaving, and select other options related to the I channel formatting/encoding. The address offset for the I channel control register is 18006 (word access). The Q channel control register is used to control data formats, select encoders, select interleaving, and select other options related to the Q channel formatting/encoding. The address offset for the Q channel control register is 10004 (word access).

4–10.10.2 The Modulator PN code offset register supports the modulator return PN codes for coherent turnaround. The modulator PN code offset register address offset is 19000. The PN generator control register is used for controlling the PN generator hardware function. The TDIF utilizes one PN code generator and provides access to the internal registers of the PN code generator as well as one PN generator control register to control PN clock phase, register mixing, enables, resets, and PN clock selects. The address offset for the PN code generator is 30000 (base) and the offset for the PN generator control register is 10002.

4 - 10.11 TDIF DACS

4–10.11.1 The TDIF has eight digital-to-analog converters (DACs) of which two are used as follows:

a. DAC1 is used for setting the power for the Q data channel. The power is set relative to the power on the I data channel.

b. DAC2 is used for setting the power for the I data channel. The power is set relative to the power on the Q data channel.

4–10.11.2 The DAC registers are set as follows for the shown power ratios:

I/Q Power Ratio	DAC 0 (I) Setting (HEX)	DAC 1 (Q) Setting
1/1	F0	F0
4/1	F0	78
1/2	AA	F0
1/4	78	F0

4 - 11 Acquisition Processor

Refer to figure 4-17 for the following ACQR functional description. The address select enables the control logic section of the ACQR by matching address lines A23-A19 of the VMEbus address with the board select bits of the P2

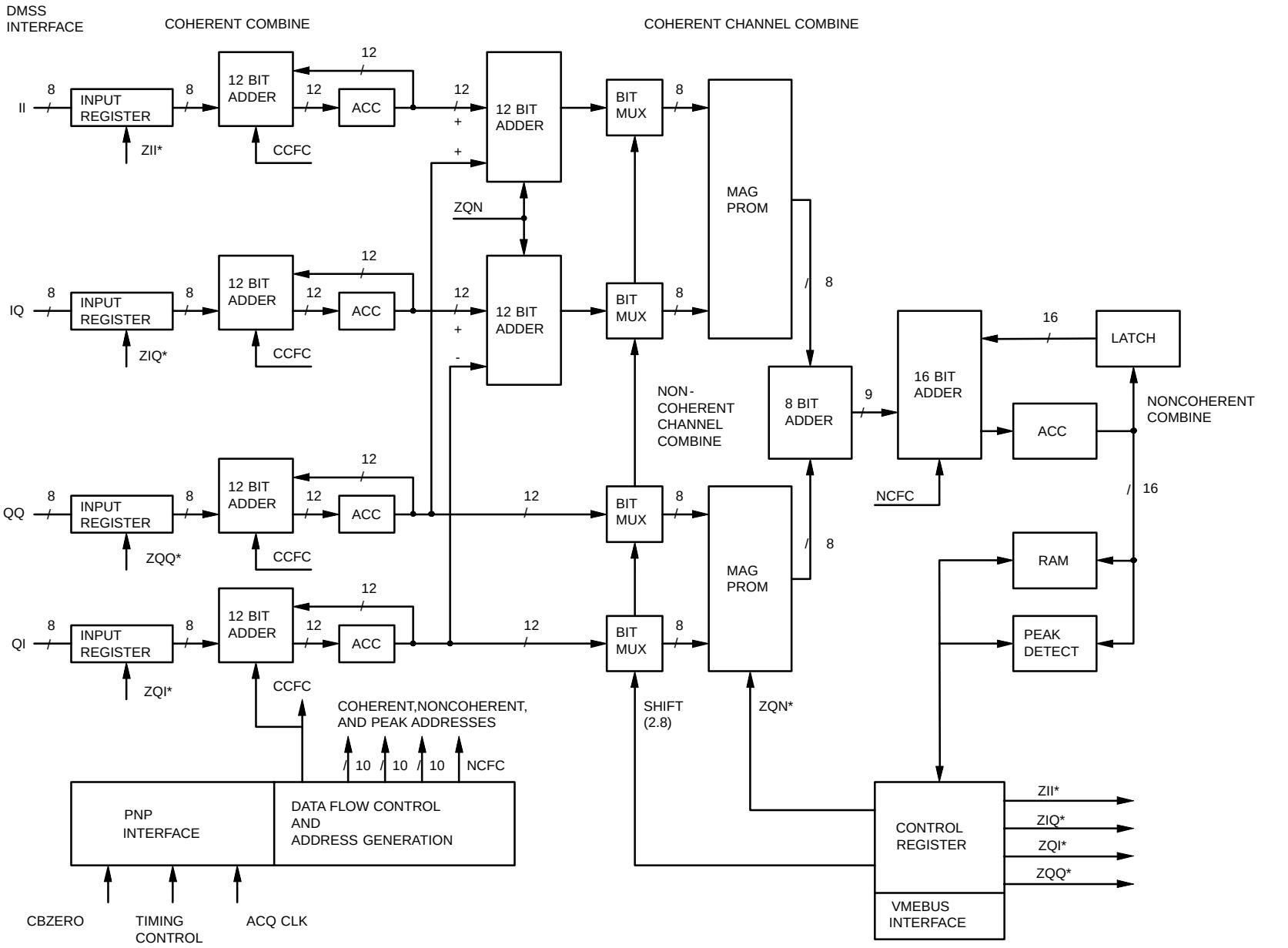


Figure 4 - 17. ACQR Functional Block Diagram

connector. The remaining 18 address lines (A18-A01) are then used by the control logic to determine the function to be processed.

4 - 11.1 VMEbus Interrupts

ACQR asserts IRQ4* following completion of the TD interval. During the interrupt acknowledge cycle, ACQR outputs a vector as programmed in the vector mask register. The following is a memory map of the ACQR:

Offset from ACQR	Base Address Function
$000 - $001	Write: Control and Vector Mask Register Read: Peak Bin Index Register
$800 - $FFF	Read: Bin Storage RAM

4 - 11.2 Acquisition Data Processing

ACQR receives 8-bit correlator sums from the DMSS. (This data is in two's complement form). The DMSS provides two sums: one for the I component of that channel, and one for the Q component. The number of coherent and noncoherent combines is determined by the timing signals coming from the PNP. The data is clocked into the ACQR with the rising edge of ACQCLK, at a rate not to exceed 6.5 MHz. See figure 4-18 for examples of the combining process within the ACQR.

4 - 11.3 Coherent Combine

Each sum is accumulated from 0 to N times, providing a coherent combination with 12 bits of resolution. N is determined by the period of TCOHB; for N greater than 15, overflow is possible for certain input signals. Accumulating zero times means that the output of this stage at time T is equal to the input at T-1. Accumulating one time means that the output is equal to the sum of the inputs at time T-L-1 and time T-1, where times T-1 and T-L-1 are in the same interval. (L is the correlator length on the DMSS.) The output of this stage is a sequence of L sums, with each sum corresponding to a correlator bin location.

4 - 11.4 Coherent Channel Combine

(Not applicable to TM) The coherent combine sums from each channel may be combined with the corresponding sum from another DMSS, (i.e., the I_I (I DMSS, I component) coherent combine sum is added to the Q_I (Q DMSS, I component) coherent combine sum, and the I_Q and Q_Q sums are similarly combined). This function is enabled or bypassed depending on the contents of the control register.

4 - 11.5 Magnitude PROMs

Only eight bits from the coherent or coherent channel combines are input to the magnitude PROMs; selection of which eight is determined by the contents of the control register. The magnitude of the signal output from the coherent (channel) combines is determined for each channel by the PROMs.

4 - 11.6 Noncoherent Channel Combine

The magnitudes of the two channels are added in this stage if the control bit in the control register is set; otherwise, the Q channel input to the adder is zeroed.

4 - 11.7 Noncoherent Combine

The outputs from the noncoherent channel combine are accumulated from 0 to N times, as determined by the PNP timing control signals. Since the input from the noncoherent channel combine may be nine bits, overflow may occur for N greater than 127 for some input signals. (The accumulated sum is 16 bits.) To minimize errors in peak detection and data processing due to overflow, output values from this stage are limited at $FFFF.

4 - 11.8 Peak Detection

Following the last noncoherent combine accumulation for an interval or subinterval, a peak search is performed in hardware. The location of the bin containing the peak value is stored in the peak bin index register.

4 - 12 PN Processor

Refer to figure 4-19 for the following PNP functional description. The address select enables the control logic section of the PNP by matching address lines A23-A19 of the VMEbus address with the board select bits of the P2 connector. The

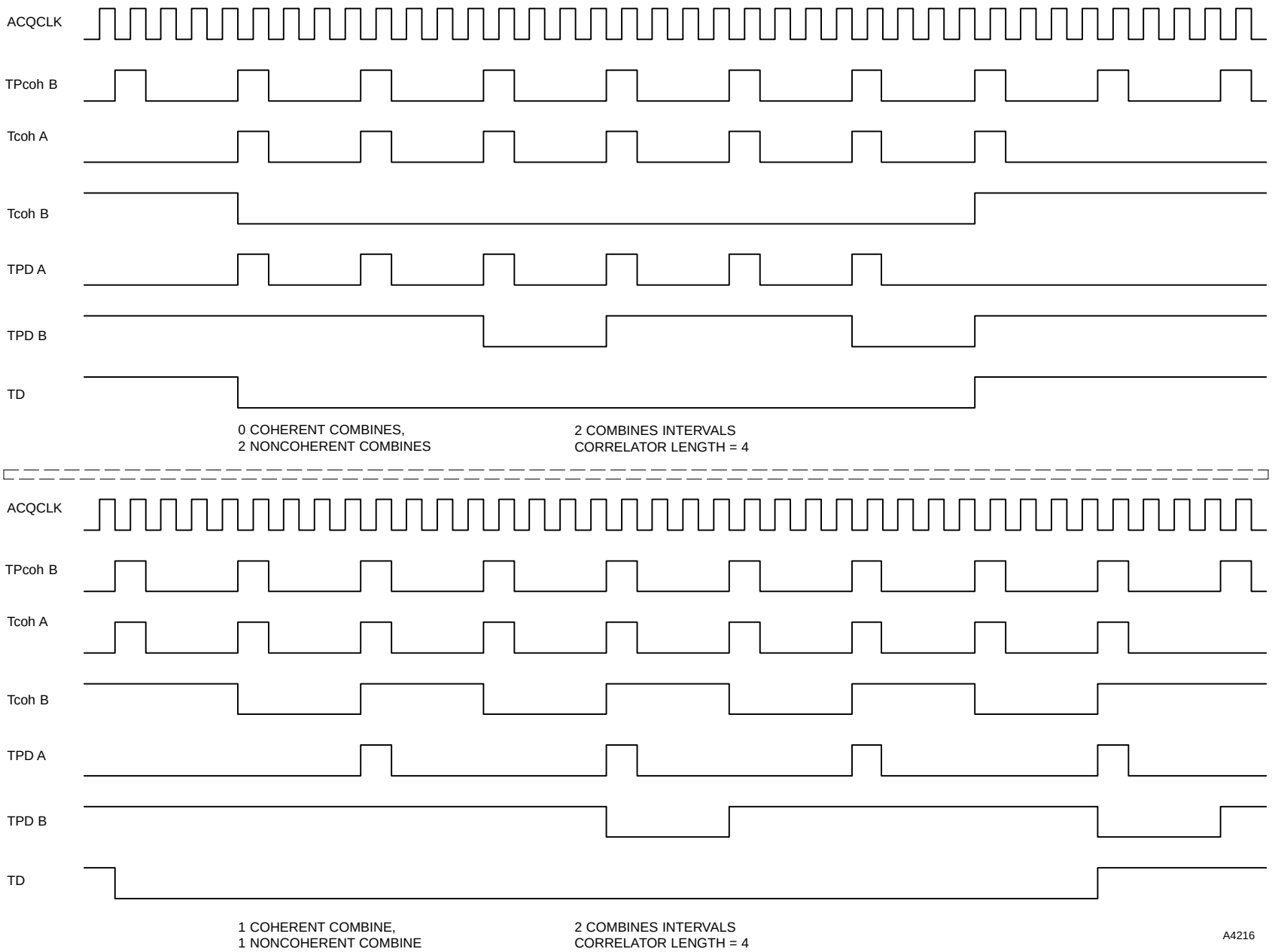


Figure 4 - 18. ACQR Timing Diagram

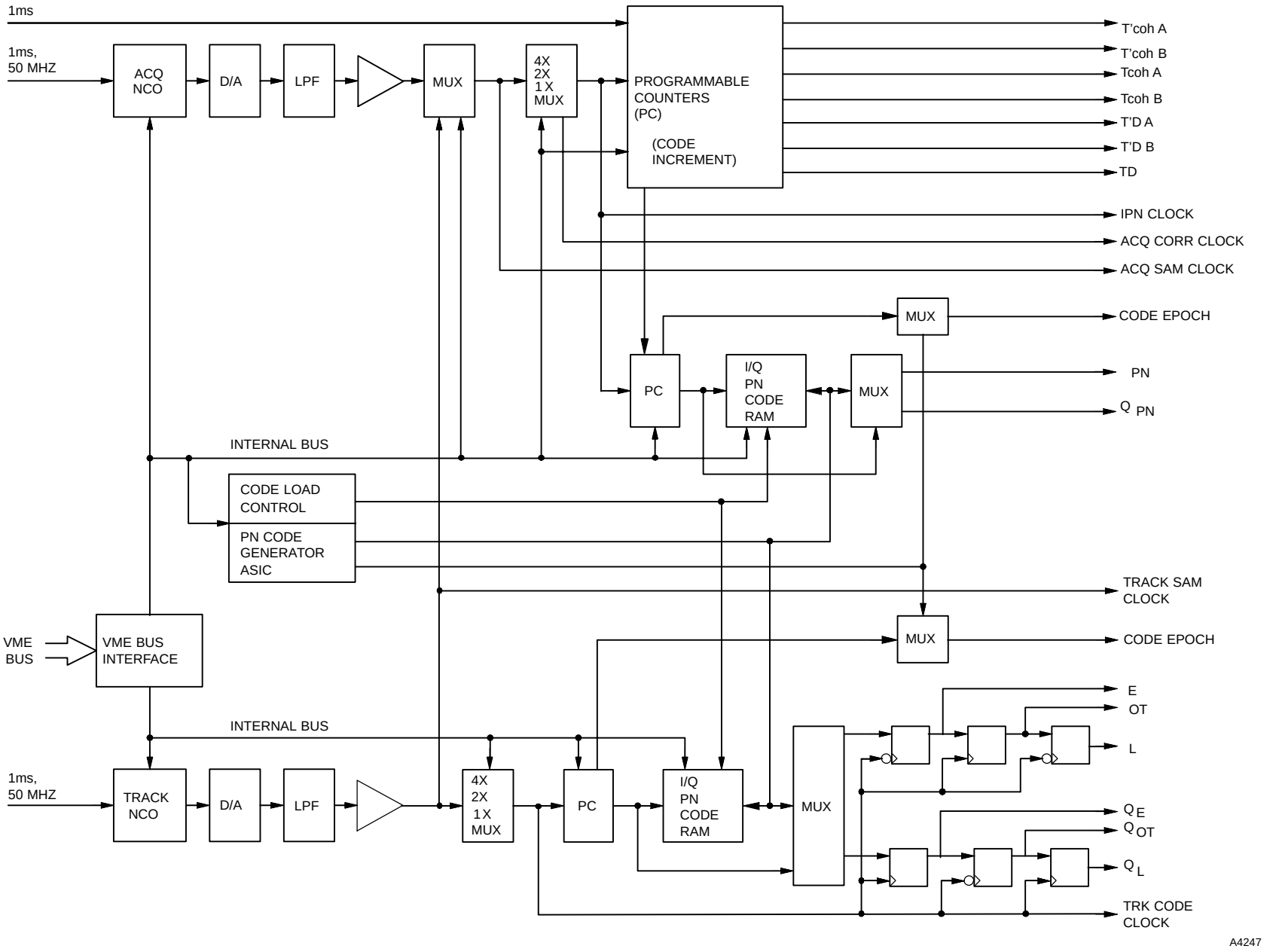


Figure 4 - 19. PNP Functional Block Diagram

remaining 18 address lines (A18-A01) are then used by the control logic to determine the function to be processed.

4 - 12.1 PN Code Generation

4–12.1.1 The PNP generates two dual PN code strings. One of the code strings is called the tracking PN code and the other is called the acquisition PN code, each having an I component and a Q component. The I part of the code is 1/2 chip ahead of the Q part. Each code string has its own NCO to control its frequency. The NCOs have a frequency range of 4 MHz to 13 MHz and can be set to run at the PN code rate, twice the code rate, or at four times the code rate.

4–12.1.2 If the PN code rate is less than 4 MHz, the codes are generated from RAM look-up tables. The PN code RAM can be loaded from the VMEbus or auto-loaded with the PN code generator chip and is adjustable from 1 to 262,144 bits in length. Both NCOs and PN code generators are updated at the 1-msec timing mark after their registers are set. Each NCO (and code generator) have an independent reset. Once the code generators are running, the code offsets are relative to the current code state. The code generators are initialized to the zero state.

Note

The maximum length registers must be set in both of the code generators before starting the auto-load function.

4–12.1.3 The tracking PN code generator generates the early, late, and ontime codes for both I and Q components. The early and late signals are half a chip off of the ontime and have a maximum skew of six nanoseconds. The acquisition PN generator outputs are inphase (within 15 nanoseconds) with the ontime outputs of the tracking PN generator, as long as both NCO's and code generators are given the same control information. If the PN code rate is higher than 4 MHz (high-rate PN), the PN code generator chip generates the output PN code directly. Only the I PN code is used in this mode. The acquisition sample clock controls the code rate in this mode.

4 - 12.2 PN Code Generator Chip

The PN code generator chip is comprised of three coders (32-bit shift-registers with programmable feedback). In the high-rate PN mode, only one of the shift-registers (coder 0) is used to generate the PN code. In the auto-load mode, coder 0 is used for the I code and coder 2 is used for the Q code. The output of coder 1 may be XORed with the output of either (or both) coder 0 and coder 2 before the PN code is stored in RAM.

4 - 12.3 Programmable Counters

4–12.3.1 The acquisition PN clock also drives four cascaded programmable counters. The four programmable counters provide timing signals for the acquisition process. See figure 4-18 for an example of the timing signals sent to the ACQR. The first counter, T'COH, has 10 bits and is set to count the length of correlators. The value set in this register is the correlator length (4-1024) minus one. The second counter, TCOH, has five bits. The value set in this register is number of coherent combines (0-31). The third counter, T'D, has 11 bits. The value set in this register is the number of noncoherent combines (0-2047). The fourth counter, TD, has seven bits. The values set in this register is the number of subintervals (1-127). When the value in this register is greater than one, the acquisition code generator is incremented by the value stored in the ACQR code increment factor register (from 0 to 1023) for each additional subinterval.

4–12.3.2 The output of bit 15 of the PNP control register drives a pin on the P2 connector and is called PN LOCK. Bit 10 of the control register controls whether the acquisition sample clock is the output of the acquisition NCO or the output of the tracking NCO (making the acquisition sample clock the same as the tracking sample clock).

4 - 13 External Clock Synchronizer

Refer to figure 4-20 for the following EXCS functional description. The address select enables the control logic section of the EXCS by matching address lines A23-A19 of the VMEbus address with the board select bits of the P2 connector. The remaining 18 address lines

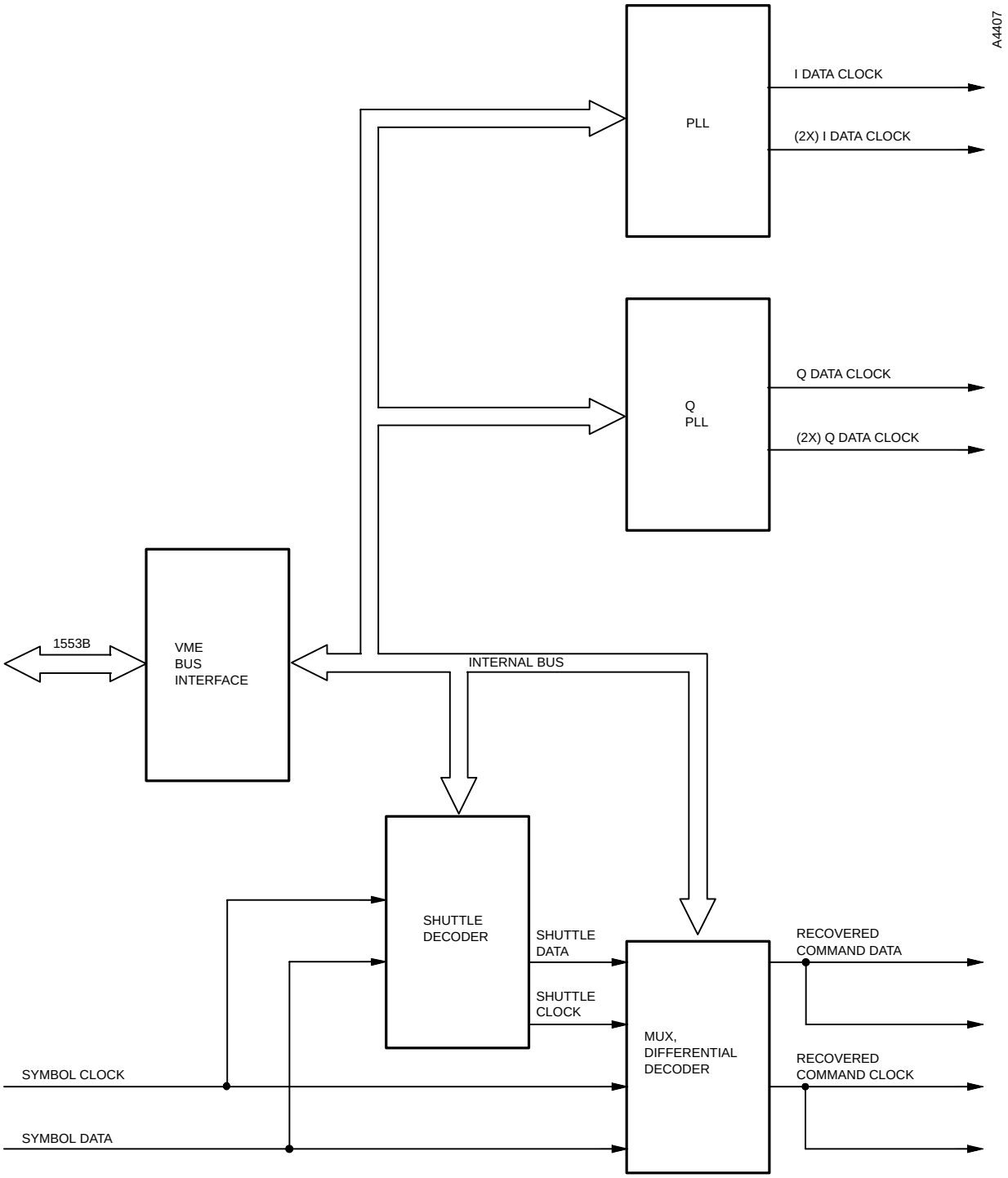


Figure 4 - 20. EXCS Functional Block Diagram

(A18-A01) are then used by the control logic to determine the function to be processed.

4 - 13.1 Shuttle Decoding

4–13.1.1 The EXCS provides the capability of outputting Shuttle decoded I symbols when enabled by control logic. The Shuttle decoder has a rate 1/3, three-bit soft-decisioned in sign magnitude, parallel loaded, Viterbi decoder with polynomial coefficients of constraint length 7 as follows:

G1 = 1111001
G2 = 1011011
G3 = 1100101

4–13.1.2 The Shuttle decoder control register must be set for proper operation of the shuttle decoding function. The disabling of the reset bit allows the Shuttle decoder function to begin synchronization. The Shuttle decoder automatically tries to synchronize itself unless the SYNCCTL bit is set. If SYNCCTL is set, the other bits in the control register are used in the manual mode in an attempt to sync.

4 - 13.2 Differential Decoding

The EXCS provides the capability of differentially decoding the command data output bits when enabled by the control logic. Differential decoding consists of converting the output bits from NRZ-S or NRZ-M to the NRZ-L format. Setting of the proper bits in the control/status register enables this function.

4 - 13.3 Phased-Locked Loops

The two PLLs are identical and have their outputs sent to the TDIF. The external clocks for the PLLs are differential TTL levels and have a frequency between 95 Hz and 12.5 MHz with a minimum pulse width of 30 nanoseconds. The PLLs do not contribute more than 2% phase jitter to the output clocks. An up/down counter is used as the phase detector. The counter uses a 50-MHz sample clock from the TIME2, keys on rising edges, and has 11 bits. If the counter sees the external clock edge first, the counter counts up (limited to 3FFh) until the local clock edge is seen. If the local clock edge is seen first, the counter counts down (limited to 400h) until the external clock is seen. When the counter stops, the NCO frequency is updated with the counter output scaled by K1. The loop is updated at the external data clock rate divided by N3, limited to a 6-MHz maximum rate.The NCO uses 22 bits and a 50-MHz reference clock, which results in an NCO frequency resolution of 11.92 Hz. The nominal frequency of the NCO is from 3 MHz to 12.5 MHz (this gives the NCO a frequency resolution of better than 0.0004%). The N1 programmable counter is used to allow the NCO to run at a higher frequency than the output clocks. The loop and the NCO have independent resets. When the loop is reset, the NCO runs at the nominal frequency; when the NCO resets, the input clocks bypass the PLL to the output. For proper operation, the NCO nominal frequency divided by N1 and N2 should be within 0.01% of the external input clock frequency. The error count of the phase detector is used to determine if the PLLs are in lock. The loop error lock level is set by the control register.

4 - 14 Demodulator Processor

Refer to figure 4-21 for the following DMDP functional description. The VMEbus address select enables the control logic section of DMDP by matching address lines A23-A19 of the VMEbus address with the board select bits of the P2 connector. The remaining 18 address lines (A18-A01) are then used by the control logic to determine the function to be processed. DMDP asserts IRQ5* following either of the VMEINT registers being accessed by TMS bus.

4 - 14.1 TMS Bus Interface

The DMDP is controlled by a digital signal processor (DSP), the TMS320C25 (TMS). Code executed by the TMS controls and receives data from the DMSS; generates interrupts to the VMEbus; sends status to the MCP over the VMEbus; receives control and configuration data from the MCP; directs the FFT controller (FFTC), a TMC2310; and loads up to eight 8-bit DACs.

4 - 14.2 Local TMS Bus

Within the local TMS bus address space, the following functions are found:

a. On-Chip Memory. This memory is zero wait-state and there are 544 words available.

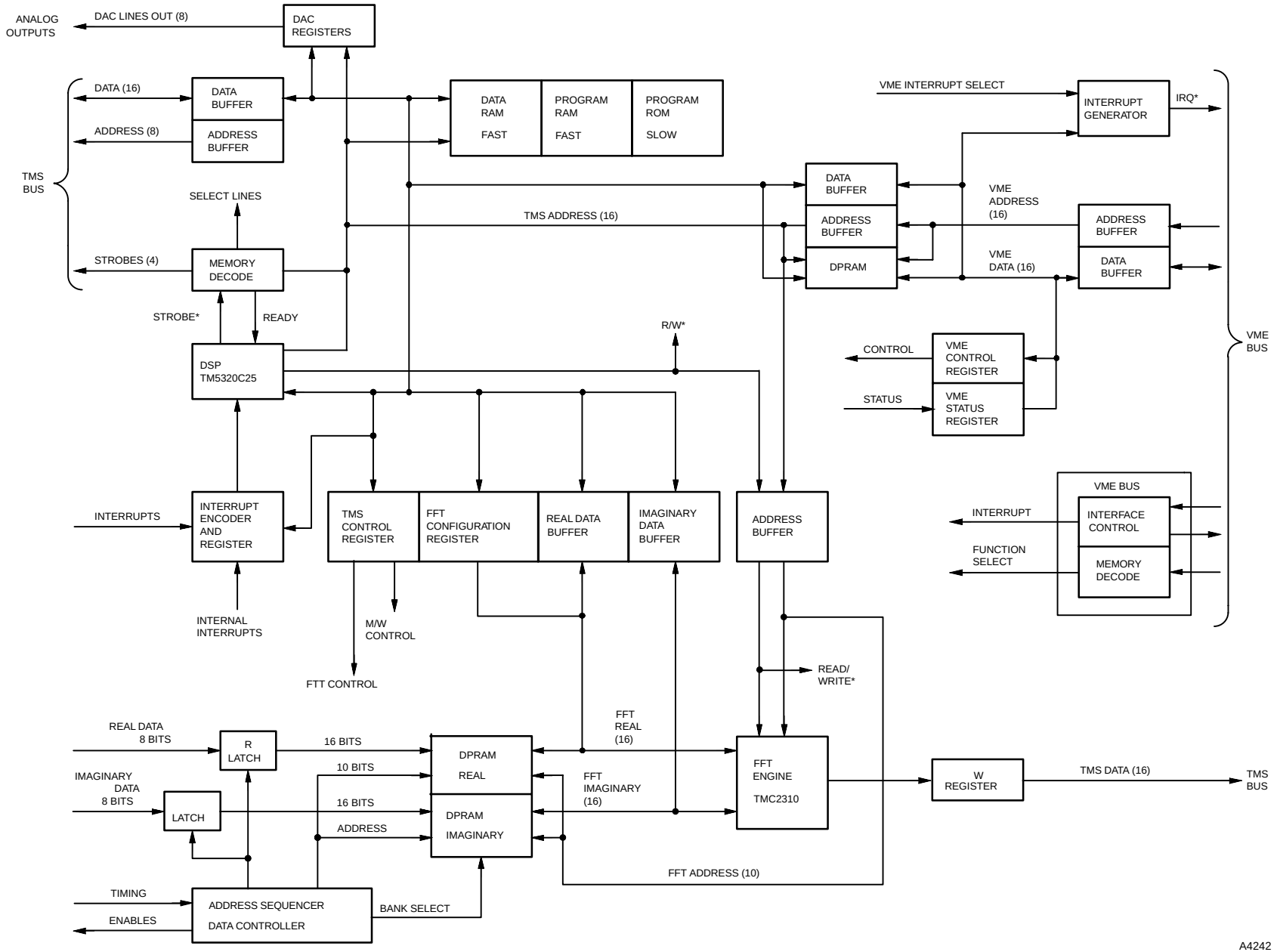


Figure 4 - 21. DMDP Functional Block Diagram

b. Off-Board Memory Space. This memory-mapped space is set up for two wait-state (<240 nanoseconds at 40 MHz) access.

c. VME Dual Port RAM (Side A). The interface with the VMEbus for passing status and control is set up for one wait-state (<140 nanoseconds at 40 MHz) access. This DPRAM is of the 2k x 16 bits size.

d. DAC Registers. Eight D/A converters are under TMS control. They appear as unique 8-bit write-only memory locations with two wait-state access. They are used to provide AGC and dc-bias compensation to the RF portion of the tracking loops. Output from each DAC is +10.0 x (VALUE/256) volts, where VALUE is the unsigned 8-bit number written to the DAC. The address offset for each DAC is the DAC number (0 through 7). (The VMEbus address offset is 2 x (DAC#).)

e. FFT DPRAM. The FFT DPRAM is size 2k complex words (2k x 2 x 16 bits). This memory also is accessible to the TMS bus as one wait-state memory when the TMS control register is configured to permit access. The memory is partitioned into 2k words each for the real and imaginary components.

f. Local Data Memory. This memory is zero wait-state access; minimum size is 4k words, with expansion capability to 32k words.

g. Program ROM. Executable code (SP7472110-XXX (J11 and J12), where XXX represents the release version) is stored in two wait-state ROM. Initialization code copies from ROM to program RAM prior to setting the RAM selection bit in the TMS control register. (This space is shared with program RAM.)

h. Program RAM. This memory is zero wait-state. When ROM is selected by the TMS control register, the actual data RAM is not accessible; program RAM occupies the same space. When RAM is selected by the control register, this RAM occupies the same space as ROM did; data RAM is then accessible.

4 - 14.3 External TMS Bus

A portion of the TMS memory space is reserved for off-board access. This space is divided into four quadrants of 256 words each; accessing a quadrant enables the corresponding STROBE signal (1-4) for controlling data transfer. This memory space is required to have memory access time of less than 240 nanoseconds (2 wait states at 40 MHz). See figure 4-22 for timing specifications.

4 - 14.4 FFT Controller Operation

The FFTC performs FFT and magnitude squared operations when directed by the TMS control register. In order to properly control the FFTC, the following sequence of operations must be performed for each function required:

a. Reset the FFTC by setting the command bit to 00b.

b. Write the first required configuration code to FFTC configuration data register (FFTCNF).

c. Load the FFTC configuration register by setting the command bits to 01b.

d. Set the command bits to 11b to deactivate the command bits.

e. Write the second required configuration code to FFTCNF.

f. Repeat steps c and d.

g. Send a start command to the FFTC by setting the command bits to 10b.

h. Repeat step d.

i. When done, the FFTC asserts a signal to generate an interrupt to the TMS.

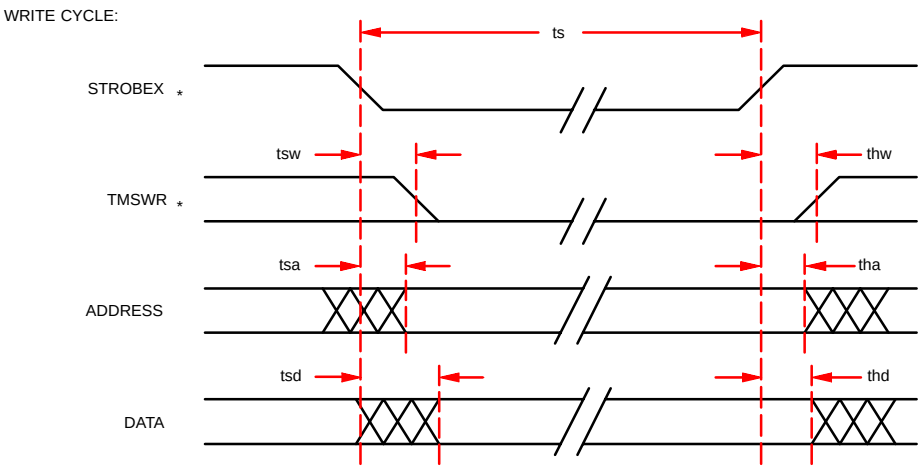
4 - 14.5 FFT Data Collection

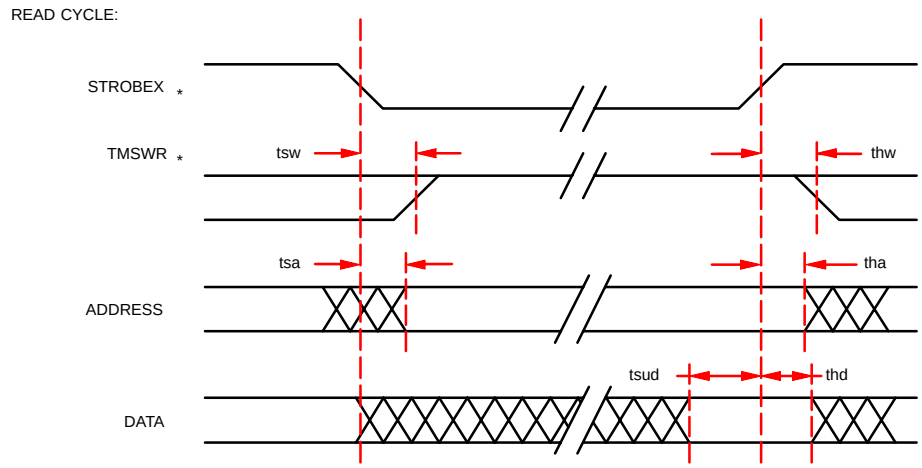
The input data to the FFT DPRAM is selected from the DMSS (I) or DMSS (Q) by the TMS control register (only DMSS (Q) is utilized by the TM). Since both sources may be selected and there is one set of input lines, the data input process is time-division multiplexed to be written into the respective memory bank in the DPRAM; DMSS (I) data to bank 1, DMSS (Q) data to bank 2. The FFT is performed in place; therefore, the data is stored in locations corresponding to the bit-reversal of the address. Data collection at rates up to 50 kHz is supported.

4 - 14.6 Zero Filling of FFT Data

Zero filling is accomplished by forcing input data sample N+1 through 2N to be identically equal to zero; i.e., samples 1 through N are input from the

A5338





TIMING SPECIFICATIONS

tsw	≤	32 ns
tsa	≤	9 ns
tsd	≤	40 ns
tsud	≥	51 ns
tha	≥	0 ns
thd	≥	0 ns
thw	≥	0 ns
ts	~	200 ns

Figure 4 - 22. TMS Bus Timing Diagram

selected DMSS, while the memory locations corresponding to samples N+1 through 2N are loaded with zero. This function is selected by the TMS control register.

4 - 14.7 VMEbus Interface

The DMDP interfaces with the VMEbus as a slave and as an interrupt generator. It uses standard addressing with a 16-bit data bus (A24:D16). Base address is selectable in 512k blocks by connecting the appropriate selection lines to ground in the unit (unused base address selection lines are pulled up to +5.0 vdc).

4 - 14.8 VMEbus Interrupts

The DMDP asserts IRQ5* following TMS access of either VMEINT register. During the interrupt acknowledge cycle, the DMDP outputs a vector to correspond with which register was accessed. Bit 1 of the vector corresponds to VMEINT1 being accessed and bit 0 of the vector corresponds to VMEINT0 being accessed. Bits 7-2 are programmable from the VMEbus by writing to the vector mask register.

4 - 14.9 VMEbus Registers

Accesses to the I/O register spaces are zero wait-state for write and one wait-state for read. Functional descriptions are listed below.

a. Hardware Control register and Vector Mask register. These registers are accessible one byte at a time, or as one word. (Bits 15-8 go to a logic zero following hardware reset; states of bits 7-2 are indeterminate following power-up).

b. TMS Interrupt Generation register (INTGEN). When this write-only register is accessed, an interrupt is generated to the TMS. This is used to indicate that new control information is present in the VME DPRAM.

c. Status register (STAT). This read-only register is available to read hardware status from DMDP.

4 - 14.10 VME Dual Port RAM (Side B)

The interface with the TMS bus for passing control status information. This DPRAM is of the 2k x 16 bits size.

4 - 14.11 Test Mode

The DMDP operates in test mode when so directed by the VME control register. In test mode, TMS operation is inhibited. The VMEbus can then logically extend onto the TMS bus for memory, functional, and closed-loop test. All accesses to the TMS bus are mapped into an appropriate space on the VMEbus.

4 - 15 Demodulator Symbol Synchronizer

Refer to figure 4-23 for the following DMSS functional description. The address strobe signal (STROBE*) enables the control logic section of the DMSS to accept the valid address input on lines TADD7-TADD0 of the TMS bus (STROBE2* enables DMSS (Q)). The 256 locations assigned to the DMSS are decoded as follows:

Address	Function
00 - 3F	Demod chip
40 - 4F	I channel acquisition correlator
50 - 5F	Q channel acquisition correlator
60 - 7F	Reserved
80	Control register 1 (write and read)
81	Control register 2 (write and read)
A0 - FF	Reserved

4 - 15.1 FIR Filters

The 8-bit digitized I and Q components of the return service signal are input to two independent finite impulse response (FIR) digital filter chips. The filters contain eight cells with nine bits of data and coefficients. The output of the filters are used for further DMSS processing or output to the other DMSS (not applicable to the TM). The filters perform the following functions:

a. The filters are able to perform decimation by the values of 1, 2, or 4. The coefficient for all decimation and bypass modes are stored in the PROM and selection is based on the mode and done by the DMDP. There are 16 sets of coefficients for each mode. There is one set of coefficients for bypass mode. The coefficients for bypass mode are stored in decimation by one section of the PROM and are all “0”s and one “1”.

b. The filters are operated in sample rates ranging from 500 ksps to the maximum of 25 msps.

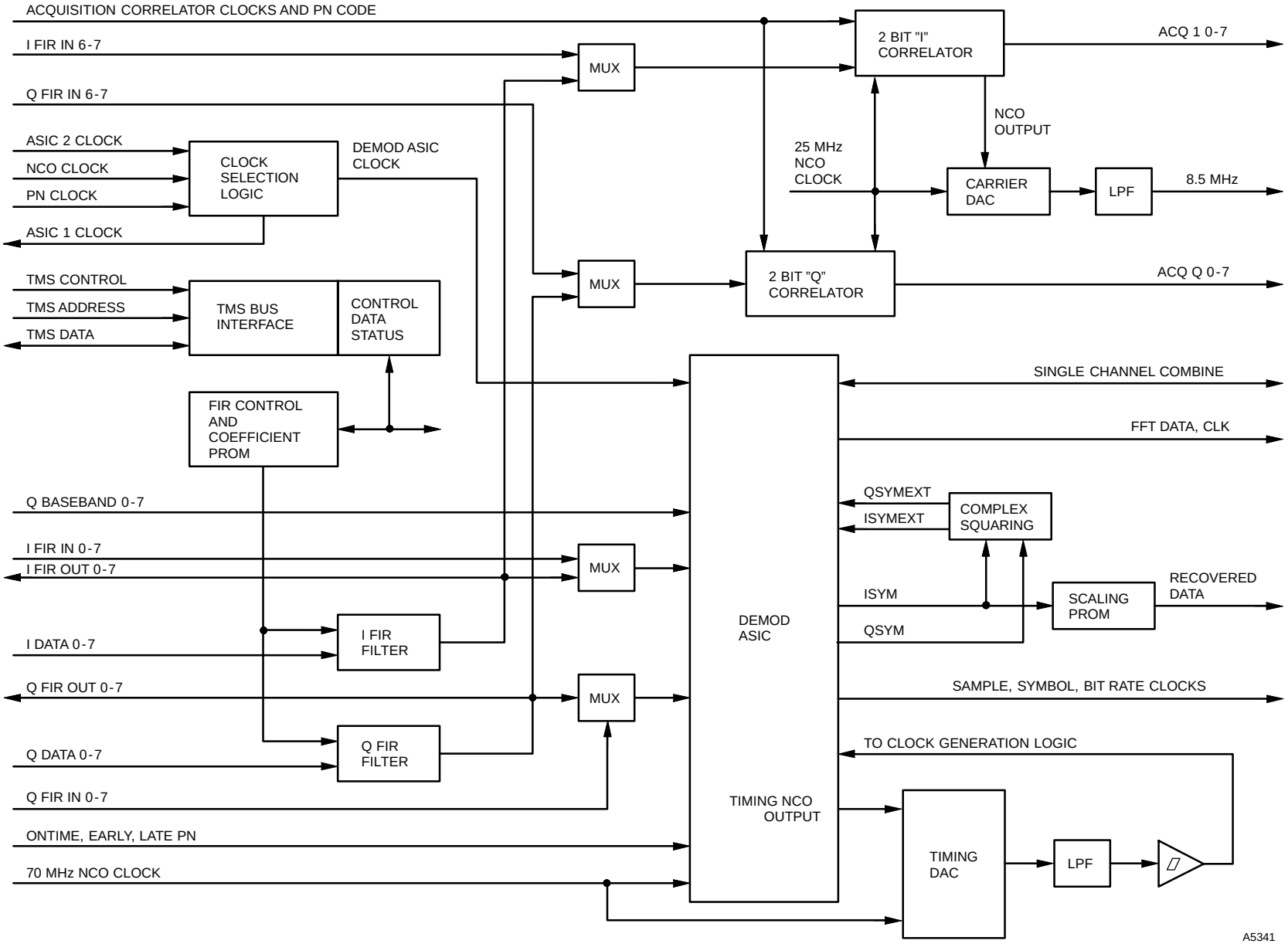


Figure 4 - 23. DMSS Functional Block Diagram

c. Output from the filters is up to 25 bits. Only eight bits from the filters are input to the Demod chip. Selection of which eight bits is determined by the value of the three control bits in control register 2.

4 - 15.2 Demod ASIC

The FIR filtered I and Q and the input baseband/subcarrier signals are processed in parallel using the Demod chip. The input to the Demod chip is either the output of the FIR filters or the input from the other DMSS (not applicable to the TM). The Demod chip performs the following functions:

a. Provides integrate-and-dump filtering, timing error detection, phase-error detection, symbol timing acquisition and tracking, timing loop filtering, and data AGC control functions for the I and Q data paths.

b. Provides PN despreading and tracking functions in the spread mode. The Demod chip also provides for the early/late PN timing error detection, noise estimation, and I/Q power level measurement.

c. There is an NCO in the Demod chip that is clocked at 70 MHz. The maximum output frequency of this NCO is 25 MHz.

d. Provides for single channel combine where the output of the single channel from one Demod chip is input to the other Demod chip of the other DMSS (not applicable to the TM). This combining process increases the signal-to-noise ratio by 3 dB.

e. The Demod chips in both DMSSs (not applicable to the TM) are synchronized together by a TMS service routine that enables both chips for synchronization on the rising edge of the 20-kHz clock.

4 - 15.3 Squaring PROMs

The six bits of I and Q data symbols, processed by the Demod chip, are passed on to a squaring PROM that performs complex squaring or quadrupling functions. There are eight sections in the PROM. One of the sections is used for squaring and the other seven sections for quadrupling functions. The DMDP selects the desired section. The real and imaginary PROM results are input to the Demod chip and after further processing, are output from the DMSS as the complex FFT data to the DMDP.

4 - 15.4 Scaling PROMs

The six bits of 2's complement I data symbols are input to a scaling PROM to perform scaling and format conversion functions. The PROM output is scaled based on the scaling factor from the TMS and converted to five bit offset binary. These five bits and the associated symbol clock are output from the DMSS in TTL logic to the EXCS. The MSB of the I symbol and symbol clock are also converted to ECL and output.

4 - 15.5 Acquisition Correlators

4–15.5.1 The DMSS contains two, multi-tap, flexible correlators, variable in length from 4-to-1024 taps to provide PN code acquisition. The correlators generate correlation values for two serial bit streams (bit 1 and bit 0). The new PN code is loaded into the correlators on the rising edge of the Tcoh clock. The inputs to the correlators are either from the FIR filters on the DMSS or from the other DMSS (not applicable to the TM). The acquisition clock signal (two times the PN clock) is used to clock two bits of I and Q data into the bit 0 and bit 1 input of the I and Q correlators. The length of the correlators is set by loading the control register in the chip. The output from the correlators for the I and Q channels are 8-bit 2's complement values that are scaled, formatted, and centered at the mid-point of the correlation output range. This value is output to the ACQR.

4–15.5.2 There is an NCO in each of the correlators. The NCO in the I channel correlator (designated as carrier NCO) is loaded by the DMDP and a 25-MHz clock is provided to clock the NCO to generate the nominal carrier frequency of 8.5 MHz. The NCO is updated based on the rising edge of the 20-kHz interrupt. The load pulse to the NCO is generated inside the correlator. The output of the NCO is converted to analog, low-pass filtered, and output on the J1 connector.

4 - 15.6 Timing Low-Pass Filter

The 8-bit output of the NCO in the Demod chip is the source of clocks used in the DMSS and throughout the TM. These eight bits are in 2's complement format. The sign bit is inverted and

the signal is input to a DAC that converts the digital data to analog at the rate of 70 MHz. The output of the DAC is fed into a seven-section 1-dB passband ripple Chebyshev low-pass filter. The cutoff frequency of the filter is 28 MHz +/- 500 kHz and the stop band attenuation is at least 40 dB.

4 - 15.7 Carrier Low-Pass Filter

The 8-bit output of the NCO in the correlator chip is the carrier frequency. These eight bits are in 2's complement format. The sign bit is inverted and the signal is input to a DAC that converts the digital data to analog at the rate of 25 MHz. The output of the DAC is fed into a five-section 0.1-dB passband ripple Elliptic low-pass filter. The cutoff frequency of the filter is 9.5 MHz +/-500 kHz and the stop band attenuation is at least 45 dB.

4 - 15.8 Clock Generation

The output of the timing low-pass filter is converted back to digital using a zero crossing detector. In non-spread mode, this clock is used to provide the system clock. In spread mode, the PN clock signal is used as the system clock. The PN clock can be either the tracking sample clock or the acquisition sample clock. The clock selection is performed based on the mode by the TMS. The system clock is input to the Demod chip and is divided down to provide all clocks required in the chip and board.

4 - 16 RF Downconverter No. 2

4–16.1 Refer to figure 4-24 for the following RFDC2 functional description. RFDC2 accepts a 370-MHz IF return service input and sends it to a bandpass filter and to a front panel test point. The nominal input 370-MHz IF signal is bandpass filtered and downconverted to a nominal 70-MHz IF through the first downconversion process. Estimated Doppler-induced frequency errors, based on available ephemeris data, are removed during this initial downconversion process under control of the digital processing portion of the TM, through Doppler-based frequency commands periodically provided for control of the 300-MHz NCO downconversion signal. The nominal 70-MHz IF signal passes through an LPF and RF amplifier before input to an RF switch. The RF switch also accepts a 70-MHz test input from the SYNTH1. The TIME1 provides the control signal determining which signal is passed. The selected 70-MHz signal is applied to a 4-way bandpass filtering network with selectable bandwidths of 0.25, 4, 8, and 16 MHz. The TIME1 provides the bandpass filtering selection control signals.

4–16.2 The filtered 70-MHz IF output is split, with one portion output to another RFDC (not applicable to the TM) and the other input to an RF switch that also accepts a 70-MHz IF signal from another RFDC (not applicable to the TM). The selected 70-MHz IF signal passes through an AGC controlled variable attenuator. The AGC signal is developed by the digital processing portion of the TM (DMDP) based on signal-plus-noise measurements, with the AGC operating point set to avoid excessive saturation of the A/D converter in the RFDC2. A tap-off of the AGC input is provided at the maintenance panel. The IF-filtered, AGC-amplified 70-MHz signal is downconverted to baseband I and Q analog signals by an I/Q mixer. The 70-MHz IF signal is also output as a test point. The I/Q mixer also accepts a 70-MHz LO signal that is developed from an 8.5-MHz NCO input from the DMSS and a fixed 61.5-MHz LO from the SYNTH1. The 8.5-MHz NCO input is synchronized to the carrier and provides the closed-loop signal processing function necessary for proper data recovery.

4–16.3 The resultant outputs from the I/Q mixer are quadrature baseband (QBB) and inphase baseband (IBB) components of the original IF input. The baseband components are low pass filtered and then input to separate RF switches which also accept a similar baseband component signal from an external source. The IBB component is also routed to a third RF switch circuit which accepts a high-rate baseband (BB) downconversion of the high-data rate IF signal from an external source. The selected baseband signals IBB and QBB are output to another RFDC (not applicable to the TM) and all three (IBB, QBB, and BB) are applied to separate A/D converters. The A/D converters utilize the sample clock from the DMSS as the sampling rate during the conversion process. The rate varies depending on the TM configuration with the sample clock less than or equal to 25 MHz. Prior to input to the A/D converters, the selected baseband component signals are offset depending on the noncoherent

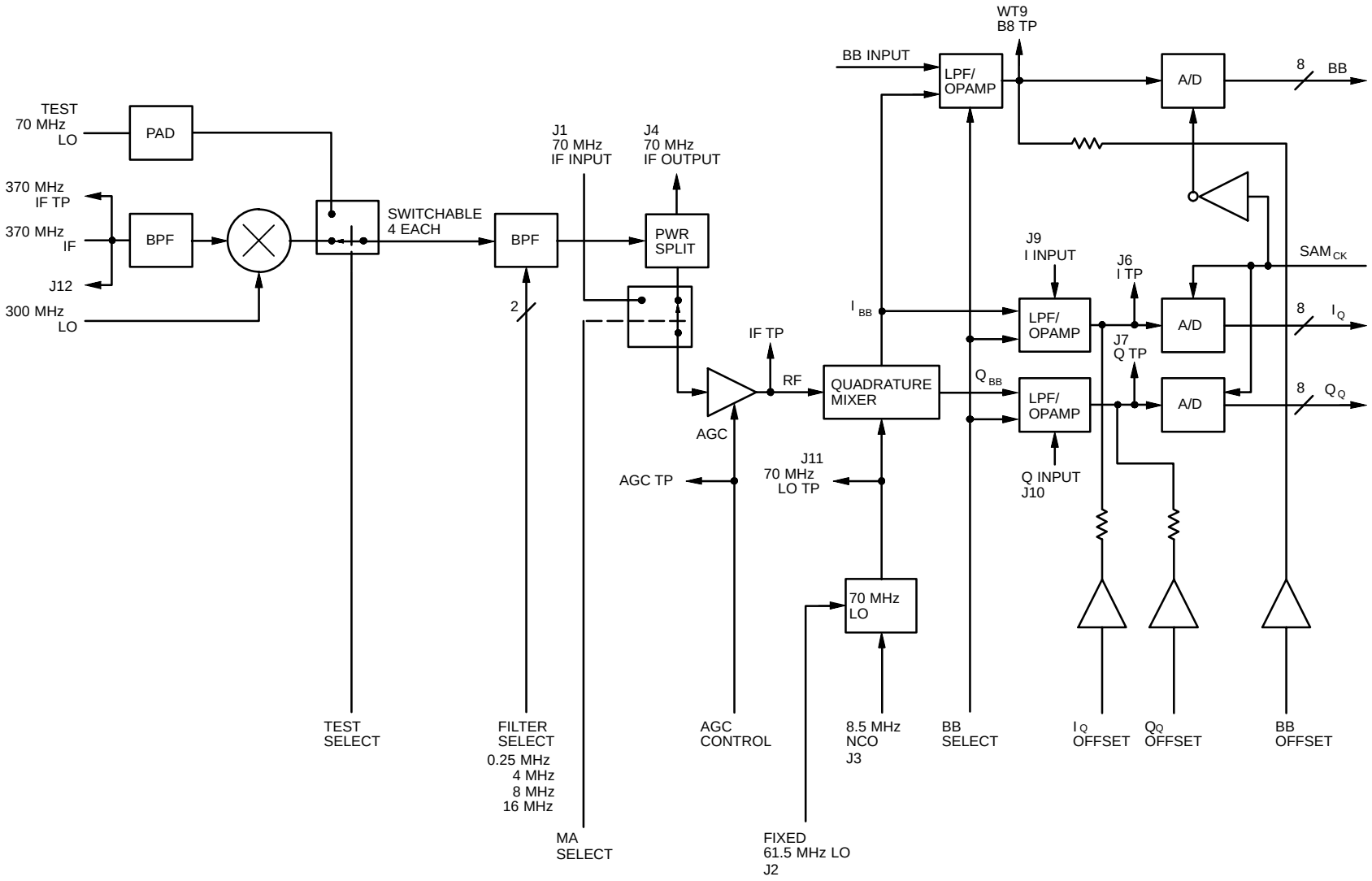


Figure 4 - 24. RFDC2 Functional Block Diagram

AGC function of the DMDP. The output of the A/D converter consists of 8-bits of baseband component data at the sample rate and are output to the DMSS.

4 - 17 Synthesizer (1 & 2).

Refer to figure 4-25 for the following SYNTH functional description. SYNTH accepts a 10-MHz reference signal from an external interface and splits it with one portion output to a test point on the maintenance panel and the other for internal processing. The 10-MHz signal is sent through a BPF with a center frequency of 10 MHz and a bandwidth of 1 MHz. The filtered signal is buffered and split with one portion for status monitoring and the other for further processing in a 140-MHz PLL. The 140-MHz PLL is performed by taking the output of a 140-MHz VCXO and dividing it by 14. The resultant 10-MHz signal is phase detected with the 10-MHz reference input. The phase error signal is put through a loop filter which drives the 140-MHz VCXO. SYNTH produces the following clocks and timing signals:

a. A 70-MHz LO signal is produced by dividing the 140-MHz phase locked signal by two.

b. A 300-MHz LO is produces by upconverting the 20-MHz NCO input using a 280-MHz signal. The 280-MHz signal is produced by multiplying the 140-MHz signal by two.

c. A 50-MHz clock is produced by adding the 20-MHz NCO input and the 10-MHz output of the divide by 14 network in the 140-MHz PLL. The resultant 30-MHz signals has a 50-MHz harmonic present which is 10 dB below the 30-MHz signal. A 50-MHz filter is used to reject the undesirable signals leaving the 50-MHz component.

d. A 61.5-MHz LO and 61.5-MHz clock are produced by high side downconverting the 61.5-MHz VCXO to 8.5-MHz using a 70-MHz produced signal. The 70-MHz signal is produced by dividing the 140-MHz PLL signal by two. The 8.5-MHz signal passed through a bandpass filter (8-MHz bandwidth) and then divided by 17 to produce 0.5 MHz. The 0.5-MHz downconversion signal which is phase compared a 0.5 MHz signal which is produced by dividing the 10-MHz (from the 140-MHz PLL) by 20. The resulting phase error output is then put through a loop filter which drives the 61.5-MHz VCXO.

e. SYNTH produces an 8.5-MHz output signal which is a direct tap-off of the 8.5-MHz signal produced in the 61.5-MHz PLL.

f. The variable 61.5-MHz LO output is produced by subtracting 8.5-MHz NCO input from the internally generated 70-MHz signal. The 70-MHz signal is produced by dividing the 140-MHz PLL signal by two.

g. SYNTH provides status by two means: (1) an LED mounted on the PWA which turns on to indicate the 61.5-MHz PLL, 140-MHz PLL, and 10-MHz reference input are correct, and (2) three output status lines indicating the same.

4 - 18 Test Modulator

Refer to figure 4-26 for the following TMOD functional description.

4 - 18.1 70-MHz QPSK Modulator

Both the I and Q data are fed to the modulator which QPSK modulates the 70-MHz LO input. An attenuator is placed in the I or Q data path for the UQPSK configuration. A switchable 70-MHz bandpass filter configuration is used at the modulator output to establish the maximum bandwidth for a range of modulation conditions (i.e., to restrict the transmitted spectrum). The available bandwidths are 1.2 MHz, 6 MHz, 12 MHz and filter bypass (effectively less than or equal to 30 MHz due to filters used in following frequency translation stages).

4 - 18.2 Eb/No Calibration

The modulated and filtered 70-MHz IF signal is routed through the Eb/No attenuator. This is a precision, digitally controlled attenuator required for Eb/No calibration purposes. The Eb/No attenuator is used in the following manner:

a. After passing through the Eb/No attenuator, the 70-MHz IF signal is output from TMOD to the noise test set (HP3708A). The HP3708A is capable of manual or IEEE-488 control.

b. The HP3708A measures the 70-MHz IF signal power present at the input using its

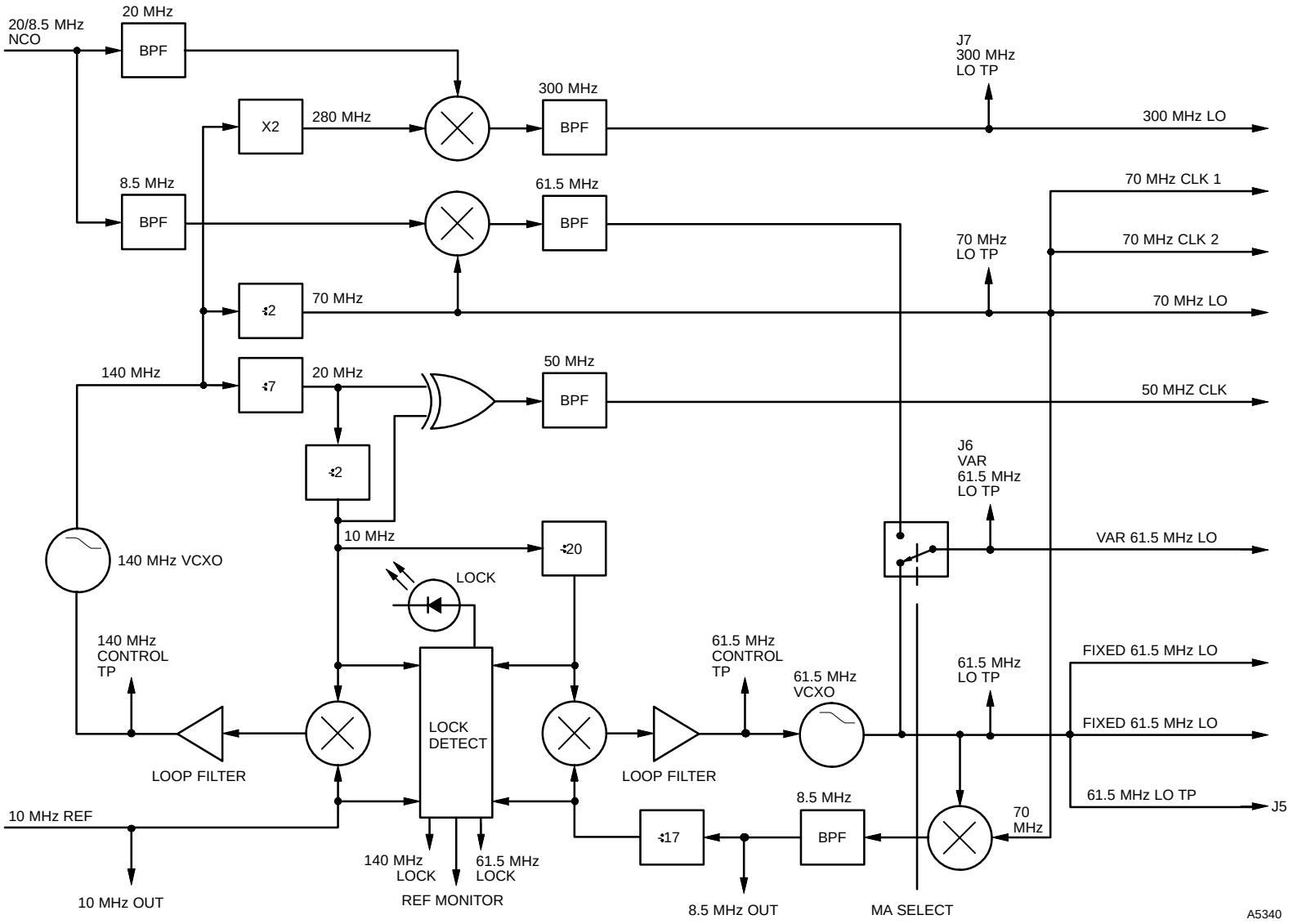


Figure 4 - 25. SYNTH Functional Block Diagram

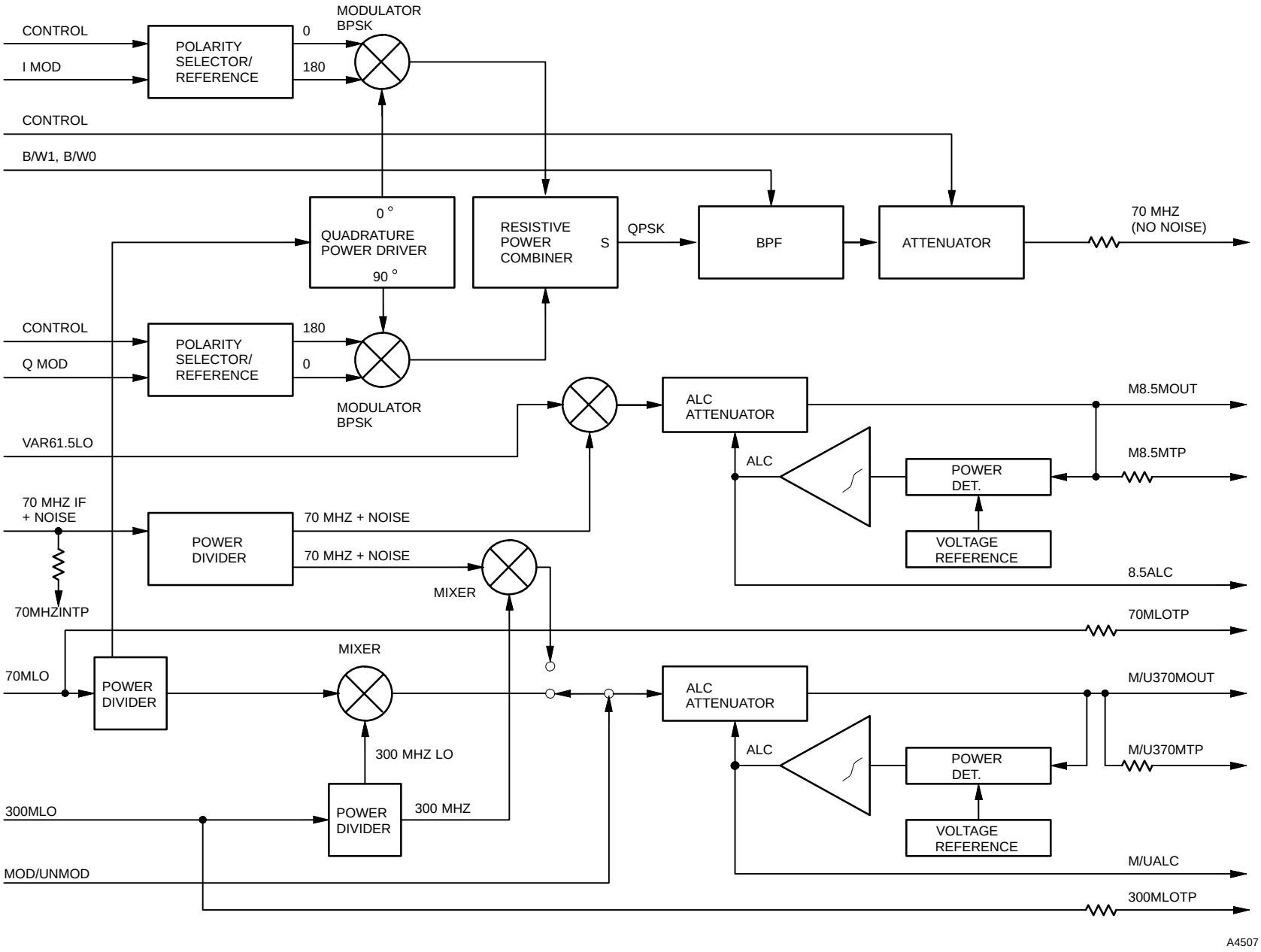


Figure 4 - 26. TMOD Functional Block Diagram

internal power meter (the bandwidth of this measurement is established by the switchable bandpass filter in the 70-MHz QPSK modulator).

c. The HP3708A sums the measured 70-MHz IF signal power with an internal precision IF noise generator. This noise source has the proper crest factor (less than 15 dB) for additive whit Gaussian noise and the noise is restricted to a known bandwidth (approximately 18 or 60 MHz). The HP3708A uses its internal power meter and table look up of the exact noise bandwidth to establish known noise power levels (N) or noise densities (No). N = 0 dBm maximum.

d. Steps (b) and (c) allow the HP3708A to accurately measure and establish carrier to noise ratios (C/N), or carrier to noise density ratios (C/No). Alternatively, energy per bit to noise density ratio (Eb/No) can be established using knowledge of the 70-MHz IF modulated bit rate. The HP3708A C/N measurements are most accurate in the -10 to +40 dB C/N range, by design.

e. The Eb/No attenuator is used in concert with the HP3708A internal power meter to calibrate and implement C/N ratios more negative than -10 dB C/N. This is accomplished by commanding the Eb/No attenuator to subtract a previously calibrated amount of the 70-MHz IF signal power (after the C/N has been established by the HP3708A (-10 to +40 dB C/N)). The Eb/No attenuator/HP3708A combination, therefore, is capable of establishing C/No ratios between 27 and 88 dB/Hz for the 18-MHz noise bandwidth and between 33 and 88 dB/Hz for the 60-MHz noise bandwidth. These ratios may be selected in 0.5 dB increments, with +/- 0.5 dB accuracy.

4 - 18.3 8.5-MHz IF Downconversion

The 70-MHz IF signal plus noise returned from the HP3708A is then split for down-conversion to the 8.5-MHz IF output. The down-conversion to 8.5-MHz IF is done by mixing the 70-MHz IF signal plus noise with the 61.5-MHz +/-85 kHz LO input. The 61.5-MHz LO is variable to allow Doppler simulation and to support MA, SSA, and KSA center frequency assignments.

4 - 18.4 370-MHz Upconversion

The upconversion to the 370-MHz IF uses the 70-MHz IF signal plus noise and the 300-MHz +/-1.6-MHz LO to produce the 370-MHz IF signals (separate modulated/unmodulated 370-MHz IF signals). Circuitry is provided for selection of the separate 370-MHz signals to permit either modulated or unmodulated 370-MHz IF outputs from the TMOD. The 300-MHz LO is variable to allow Doppler simulation and to support MA, SSA, and KSA center frequency assignments.

4 - 18.5 Automatic Level Control

Separate automatic level control (ALC) circuits are provided for the 8.5-MHz and 370-MHz IF outputs. A common ALC circuit is used for the select 370-MHz IF modulated or unmodulated output. The ALC circuits provide an optimum 0 dBm IF output level.

4 - 19 Touch Panel Display

Refer to figure 4-27 for the following touch panel display functional description. The touch panel display scans the front panel switch rows until either a serial input is received or a switch closure is detected. If a serial input is received, switch scanning is suspended until the input is processed. If a switch closure is detected, then the closed row number is stored in a register and the columns are scanned to find the closed column. The switch data is then sent to the MCP.

4 - 19.1 Switch Matrix

The switch matrix is composed of infrared emitter/sensor pairs. These pairs are on opposite edges of the display (side to side and top to bottom). Scanning starts by turning on an emitter and enabling its corresponding sensor. If the sensor receives the emitter signal, the switch is not closed and scanning proceeds to the next emitter/sensor pair. A microprocessor controls the switch overlay and serial communications (which include display inputs and switch outputs). In the serial mode, data first goes to the microprocessor and is then converted to a parallel format before being sent to the display. Conversely, in the parallel mode, ASCII data is sent directly to the display input port and switch data comes from the microprocessors's parallel output. This is why it is necessary to

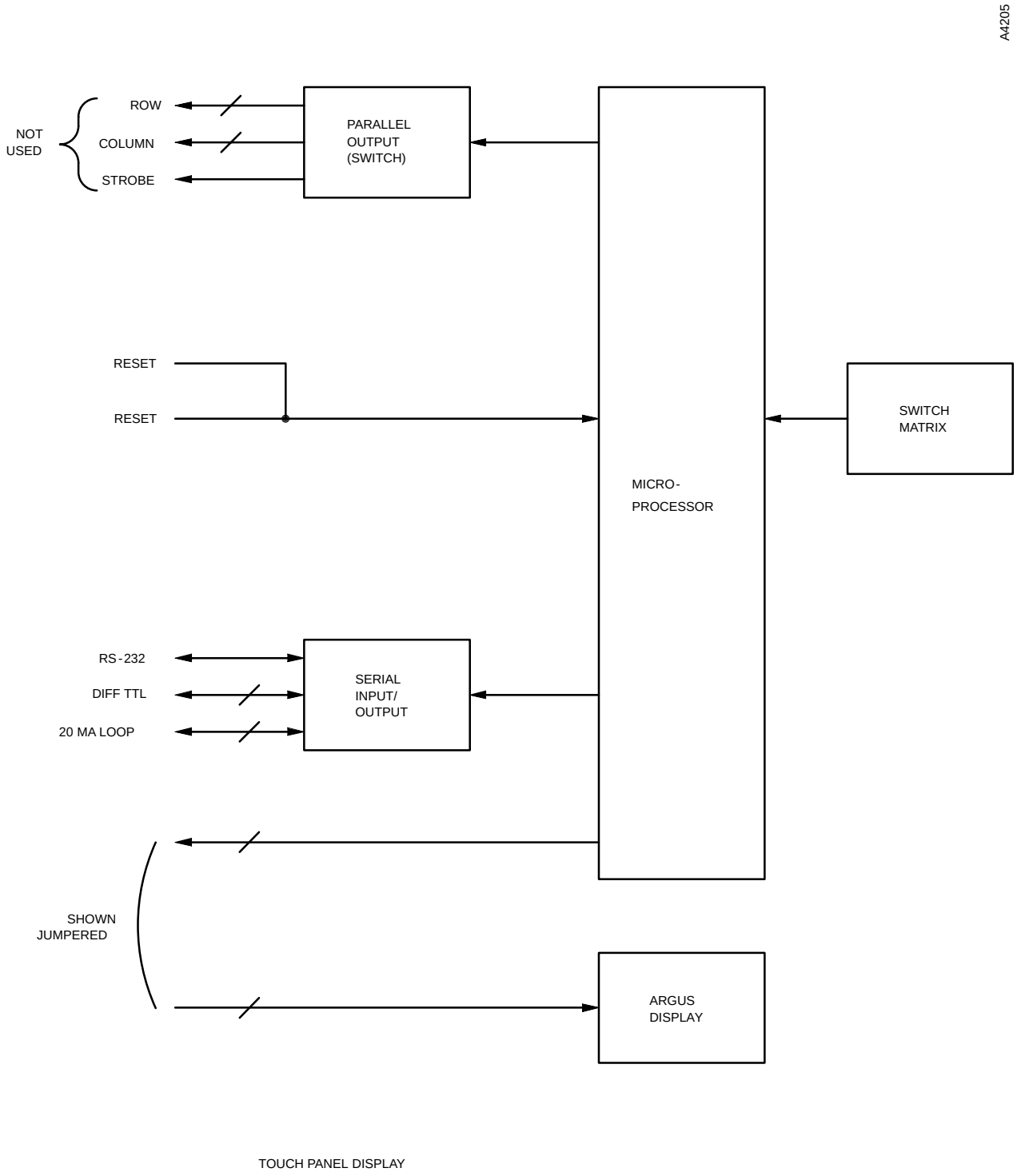


Figure 4 - 27. Touch Panel Display Functional Block Diagram

have a jumper cable installed for serial operation and removed for parallel operation.

4 - 19.2 Switch Selectable Options

Many of the switches used to select options are read only on power-up and reset. It is therefore required that after changing any switch setting, a power-up or reset must be initiated. In some cases (eg., single touch/multi-touch) the switch settings become power-up default conditions for software alterable functions.

4 - 19.3 Blanking/Dimming

The touch panel display has a combination blanking/dimming input. It can be used for blanking, dimming, both, or neither. For no blanking or dimming, no connection is to be made to the input. For dimming only, connect a 25K potentiometer in series with a 1.5K resistor between VCC (+5 vdc) and the blanking/dimming input. Maximum brightness occurs when maximum resistance is in the circuit. For blanking only, place a 1K resistor between VCC and the blanking/dimming input. For a combination, connect both circuits previously mentioned.

4 - 19.4 Reset

Holding this input to a low for a minimum of 20 milliseconds resets the unit to its initial condition and load all DIP switch programmed settings into the touch panel display controller.

4 - 19.5 Test Switch

The test switch on SW1 must be OFF at all times. If left ON, switch matrix scanning continues despite interruption of an infrared beam. This switch is used only for testing and set-up.

4 - 19.6 Switch Output

Switch ME1 controls the switch output offset. With ME1 in the OFF position, row data is output as rows 0 thru 11, column data is output as 0 thru 19. When ME1 is in the ON position, row data is output as 1 thru 12, column data as 1 thru 20. ME2 controls how many switch position can be touched at the same time. ME2 in the OFF position inhibits output switch data when two or more touch switch position are closed at the same time. ME2 in the ON position allows the first scanned switch to be output when two or more are closed at the same time.

4 - 19.7 Beeper

The beeper is enabled by placing the BP switch in the OFF position. The beeper is disabled when the BP switch is in the ON position. After the beeper is enabled, it beeps when a switch closure is detected or when an ASCII 07 (BEL) is sent in the serial mode.

4 - 19.8 Self Test

A partial self test is enabled by placing a jumper wire from pin 2 to pin 3 of the serial connector (J2). With this jumper installed, a closed switch position is displayed on the display in the following format: “@, 2-character row number, 2-character column number.” For example, if ME1 is ON and the top row, left column switch is closed, the unit display “@0101”. A closed switch at the bottom row, left column displays “@1201”.

4 - 20 Test Modem External Interface Description

Refer to table 4-1 for a description and connector pin identification of the external interfaces for the Test Modem.

4 - 21 Test Modem Internal Interface Description

During Level 1 maintenance, the only accessible internal interface signals are located on the maintenance panel and described in section 3, table 3-2. Remaining internal interface signals are not applicable to Level 1 maintenance; therefore, this paragraph is not applicable.

4 - 22 Mechanical Components

This paragraph is not applicable to the Test Modem.

Table 4 - 1. External Interface Signals

CONNECTOR	PIN	MNEMONIC	DESCRIPTION
J101	A B C	115VAC CHASSIS GMD 115VAC RTM	Site-supplied source power.
J102	1 2	70 MHZ IF IN SHIELD	Loopback of 70-MHz IF output signal; input from noise test set with selected noise added.
J103	1	70 MHZ IF OUT	70-MHz IF signal output to noise test set for noise addition.
J104	1 2	IBCLK IBCLKG	I channel clock output to I BERT. I channel clock ground.
J105	1 2	QBLCK QBCLKG	Q channel clock output to Q BERT. Q channel clock ground.
J106	1 2	CBCLK CBCLKG	Command channel clock output to Command BERT. Command channel clock ground.
J107	01 02 09 05 06 14 03 04 10	EXTIDAT+ EXTIDAT - SHIELD EXTQDAT+ EXTQDAT - SHIELD EXTICLK+ EXTICLK - SHIELD	I channel external data input. This input data is optionally formatted, encoded, interleaved, and/or spread if external data is selected as the data source. Return. Q channel external data input. This input data is optionally formatted, encoded, interleaved, and/or spread if external data is selected as the data source. Return. External I clock input from HWCI-differential TTL levels. Used to clock external I data when selected. Return.

Table 4 - 1. External Interface Signals (Continued)

CONNECTOR	PIN	MNEMONIC	DESCRIPTION
J107 (cont'd)	07	EXTQCLK+	External Q clock input from HWCI-differential TTL levels. Used to clock external I data when selected.
	08 15	EXTQCLK - SHIELD	Return.
J108	01	CRECDAT_	Command recovered data output to HWCI. Differentially driven TTL output levels.
	02 09	CRESDAT - SHIELD	Return.
	03	CRECCLK+	Command recovered clock output to HWCI. Differentially driven TTL output levels.
	04 10	CRECCLK - SHIELD	Return.
J109	08	IRECDATA+	I recovered data from IR. Converted to single ended TTL, buffered, and output to I BERT.
	09 23	IRECDATA - SHIELD	Return.
	10	IRECCLK+	Recovered I clock input from IR. Buffered and sent to I BERT to clock I recovered data.
	11 24	IRECCLK - SHIELD	Return.
	12	QRECDATA+	Q recovered data from IR. Converted to single ended TTL, buffered, and output to Q BERT.
	13 25	QRECDATA - SHIELD	Return.
	14	QRECCLK+	Recovered Q clock input from IR. Buffered and sent to Q BERT to clock Q recovered data. Return.
	15 16	QRECCLK - SHIELD	Return.

Table 4 - 1. External Interface Signals (Continued)

CONNECTOR	PIN	MNEMONIC	DESCRIPTION
J109 (cont'd)	01 02 03 04 05 06 07	RTADA0 RTADA1 RTADA2 RTADA3 RTADA4 RTADAP RTADAR	1553 Bus TM remote terminal address select inputs.
J110	01 02 09 03 04 10	LDRDAT+ LDRDAT - SHIELD LDRCLK+ LDRCLK - SHIELD	Low data rate output data channel that supports KSA split modes. The high data rate (HDR) PTE is the end user. Return. Symbol clock (and 2X symbol clock for biphase formats) for the LDR channel data output. This clock is not related to PN modulated data on the LDRDAT signals for spread modes and is thus only valid for unspread data. Return.
J111	08 09 25 10 11 26 01 02 03 04 05 06 07	CDATAO+ CDATA0 - SHIELD CCLKO+ CCLKO - SHIELD RTA0 RTA1 RTA2 RTA3 RTA4 RTAP RTAR	Command (test) data output to MDP. This is differ - ential TTL baseband Command test data that is a reclocked version of the Command BERT data input. Return. Command (test) data clock output to MDP. Return. 1553 Bus TM remote terminal address select inputs.

Table 4 - 1.sExternal Interface Signals (Continued)

CONNECTOR	PIN	MNEMONIC	DESCRIPTION
J112	01	DIO1*	I488 bus data bit 1.
	02	DIO2*	I488 bus data bit 2.
	03	DIO3*	I488 bus data bit 3.
	04	DIO4*	I488 bus data bit 4.
	05	EIO*	End or identify.
	06	DAV*	Data valid.
	07	NRFD*	Not ready for data.
	08	NDAC*	Not data accepted.
	09	IFC*	Interface clear.
	10	SRQ*	Service request.
	11	ATN*	Attention.
	12	SHIELD	
	13	DIO5	I488 bus data bit 5.
	14	DIO6*	I488 bus data bit 6.
	15	DIO7*	I488 bus data bit 7.
	16	DIO8*	I488 bus data bit 8.
	17	REN*	Remote enable.
	18	GND1	Ground.
	19	GND2	Ground.
	20	GND3	Ground.
	21	GND4	Ground.
	22	GND5	Ground.
	23	GND6	Ground.
	24	GND7	Ground.
J113	1	IJITIN	I channel jitter clock input. This clock is used as an external clock input that is used for jitter tests.
	2	SHIELD	
J114	1	QJITIN	Q channel jitter clock input. This clock is used as an external clock input that is used for jitter tests.
	2	SHIELD	
J115	1	IDATA	I channel data input from I BERT.
	2	IDATAG	I channel data ground.
J116	1	QDATA	Q channel data input from Q BERT.
	2	QDATAG	Q channel data ground.
J117	1	CDATAI	Command channel data input from Command BERT.
	2	CDATAIG	Command channel data ground.

Table 4 - 1. External Interface Signals (Continued)

CONNECTOR	PIN	MNEMONIC	DESCRIPTION
J118	1 2	8.5MHZIF SHIELD	8.5-MHZ IF subcarrier output to HWCI.
J119	1 2	M/U370MHZ SHIELD	Modulated/unmodulated 370-MHz IF output to HWCI.
J120	1 2	IRD2BRT IRD2BRTG	I channel recovered data output to I BERT. Represents the demodulated data received via the IRECDATA+/ - inputs. Converted to single ended TTL, buffered, and output to I BERT. I channel recovered data ground.
J121	1 2	QRD2BRT QRD2BRTG	Q channel recovered data output to Q BERT. Represents the demodulated data received via the QRECDATA+/ - inputs. Converted to single ended TTL, buffered, and output to Q BERT. Q channel recovered data ground.
J122	1 2	CRD2BRT CRD2NBRTG	Command channel recovered data output to Command BERT. Represents the demodulated command data received via the symbol synchronization processes. Converted to single ended TTL, buffered, and output to Command BERT. Command channel recovered data ground.
J123	1 2	IRC2BRT IRC2BRTG	I channel recovered data clock output to I BERT. Represents the demodulated data received via the IRECCLK+/ - inputs. Converted to single ended TTL, buffered, and output to I BERT. I channel recovered data clock ground.
J124	1 2	QRC2BRT QRC2BRTG	Q channel recovered data clock output to Q BERT. Represents the demodulated data received via the QRECCLK+/ - inputs. Converted to single ended TTL, buffered, and output to Q BERT. Q channel recovered data ground.

Table 4 - 1. External Interface Signals (Continued)

CONNECTOR	PIN	MNEMONIC	DESCRIPTION
J125	1 2	CRC2BRT CRC2BRTG	Command channel recovered data clock output to Command BERT. Represents the demodulated command data clock received via the symbol synchronization processes. Converted to single ended TTL, buffered, and output to Command BERT. Command channel recovered data clock ground.
J126	1 2	MA SHIELD	Not used.
J127	1 2	370MHQIN SHIELD	370-MHz IF input from HWCI.
J128	1 2	10MHZIN1 SHIELD	10-MHz reference signal from CTFS.
J129	1 2	1PPS SHIELD	1-Hz reference signal from CTFS.
J130	1 2	IRIGB SHIELD	Unmodulated IRIG-B (time of year) input from CTFS.
J131	1 2 3	1553 BUS 1553 BUS RTN SHIELD	MIL-STD-1553B digital time division command/ response multiplex data bus (A1).
J132	1 2 3	1553 BUS 1553 BUS RTN SHIELD	MIL-STD-1553B digital time division command/ response multiplex data bus (A2).
J133	1 2 3	1553 BUS 1553 BUS RTN SHIELD	MIL-STD-1553B digital time division command/ response multiplex data bus (B1).
J134	1 2 3	1553 BUS 1553 BUS RTN SHIELD	MIL-STD-1553B digital time division command/ response multiplex data bus (B2).

This Page Intentionally Left Blank

Section 5 – Maintenance

5–1 Introduction

5–1.1 This section contains information to aid personnel in the Level 1 maintenance of the Test Modem. Level 1 maintenance is defined as those tasks permitting a technician (with the unit installed in the equipment rack) to fault isolate a failure to the chassis line replaceable unit (LRU), remove and replace the faulty LRU, and restore the unit to operation within a specified time. Major component LRUs are listed in table 5-1. Before performing any procedures, refer to paragraph 3-5 for warnings aimed at preventing death or injury and equipment damage.

5–1.2 Level 2 maintenance instructions are not provided for in this manual. Level 2 maintenance is defined as those tasks permitting a technician (with the unit removed from the equipment rack and taken to the HMD area) to fault isolate the failure to the LRU. Repairable LRUs are sent to the depot for repair. Depot level maintenance consists of repairing failed LRUs to the piece part, repairing any other discrepancy not discovered at the Level 1/2 maintenance level, equipment refurbishment and performing major modifications to the equipment, when required. The TM manufacturer maintains depot maintenance facilities for all LRUs. Refer to table 5-2 for the TM maintenance concept.

5–2 Performance Standards

Minimum performance standards for Level 1 operation and maintenance are detailed in paragraph 5-6 operational verification. If the TM fails to meet any of the procedural performance steps, perform TM fault isolation procedures (paragraph 5-4).

5–3 Test and Adjustment Procedures

Test and adjustment procedures for the TM include only power supply adjustments. The following procedure describes how to adjust PS1 and PS2.

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

d. Applying pressure to bottom cover towards unit chassis, use a flat-tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

e. Carefully lower bottom panel to gain access to power supplies.

f. Refer to the following list of voltage adjustments and figures 5-1 and 5-2 for location of adjustment potentiometers when performing power supply voltage adjustments.

Power Supply	Adjustment	Test Point	Voltage
PS1	V - ADJ#1	+5	+5.0 +/ - 0.25 Vdc
PS1	V - ADJ#2	+15	+15.0 +/ - 0.5 Vdc
PS1	V - ADJ#3	- 15	- 15.0 +/ - 0.5 Vdc
PS1	V - ADJ#4	+5RF	+5.0 +/ - 0.25 Vdc
PS2	V1	- 5.2	- 5.2 +/ - 0.25 Vdc
PS2	V2	+12	+12.0 +/ - 0.25 Vdc
PS2	V3	- 12	- 12.0 +/ - 0.25 Vdc

WARNING

When adjusting voltages, beware of power terminals. Voltage present may cause DEATH or injury.

Table 5 - 1. Replaceable LRUs

NOMENCLATURE	PART	LRU	LEVEL
Test Modem	7472500		
Timing Generator	7473000 - 502	X	1, 2
Demodulator/Symbol Synchronizer	7473100 - 502	X	1, 2
Acquisition Processor	7473200 - 501	X	1, 2
PN Processor	7473300 - 501	X	1, 2
Modem Control Processor	7473600	X	1, 2
RF Downconverter No. 2	7474300 - 500	X	1, 2
Synthesizer	7474600 - 500	X	1, 2
Demodulator Processor	7476100	X	1, 2
488 Interface Control	7473700	X	1, 2
Test Data Interface	7473900 - 501	X	1, 2
External Clock Synchronizer	7510400 - 501	X	1, 2
Test Modulator	7475000 - 500	X	1, 2
Power Supply No. 1	LFQ - 27 - 1	X	1, 2
Power Supply No. 2	RMV223B - 2330 - 0450	X	1, 2
Power Supply No. 3	7516900	X	1, 2
Tubeaxial Fan	A47 - B15A - 15T3 - 000	X	1, 2
Lamp Cartridge (green, DS1 only)	CF296CWPG6 - 120VAC - B	X	1, 2
Lamp Cartridge (green)	507 - 4857 - 3732 - 500	X	1, 2
Lamp Cartridge (red)	507 - 4757 - 3731 - 500	X	1, 2
Lamp Cartridge (amber)	507 - 4957 - 3733 - 500	X	1, 2
Touch Panel Display	7519500	X	2
Lampholder	DH0 - 30Y - D86BWC	X	2
Pushbutton Switch	W403PGR	X	2
Toggle Switch (AC POWER)	MS24659 - 22F	X	2
Toggle Switch (LOCAL/REMOTE)	MS24658 - 23F	X	2
Circuit Breaker	MS25244 - 10	X	2
RF Coaxial Switch	8021 - A35 - A4B - 1C0	X	2
Harness Assembly	7472560	X	2

Table 5 - 2. Maintenance Concept

LEVEL 1 MAINTENANCE	LEVEL 2 MAINTENANCE	DEPOT LEVEL
TASK	TASK	TASK
• Detect malfunctions • Isolate LRU • Remove/replace LRU • Preventive maintenance	• Localize fault to subassembly • Isolate LRU • Remove/replace LRU • Preventive maintenance	• Repair LRU
Timing Generator		Repair
Demodulator/Symbol Synchronizer		Repair
Acquisition Processor		Repair
PN Processor		Repair
Modem Control Processor		Repair
RF Downconverter No. 2		Repair
Synthesizer		Repair
Demodulator Processor		Repair
488 Interface Control		Repair
Test Data Interface		Repair
External Clock Synchronizer		Repair
Power Supply No. 1		Repair
Power Supply No. 2		Repair
Power Supply No. 3		Repair
Lamp Cartridges (all) - Discard		
Tubeaxial Fan - Discard		
	Harness Assembly	Repair
	Touch Panel Display	Repair
	Lampholders (all) - Discard	
	Front Panel Switches - Discard	
	Circuit Breaker - Discard	
	RF Coaxial Switch - Discard	

g. Set AC POWER ON/OFF switch to ON.

h. Connect digital voltmeter to respective power supply voltage test point on the maintenance panel and adjust voltage to within specifications. If specifications cannot be achieved, replace faulty power supply and repeat this procedure.

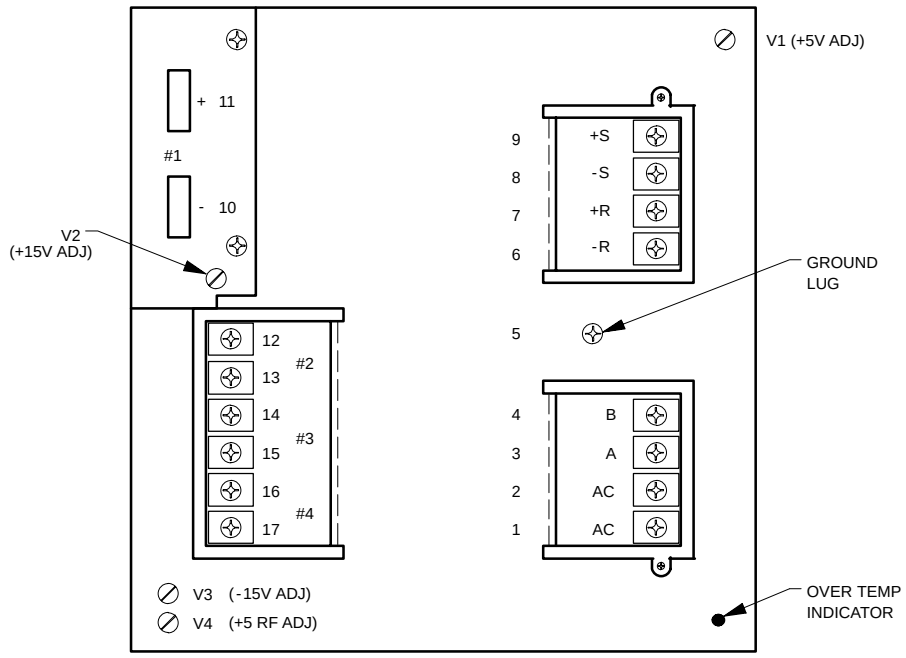
i. Set AC POWER ON/OFF switch to OFF.

j. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

k. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

l. Tighten four front-panel captive screws to the cabinet assembly.

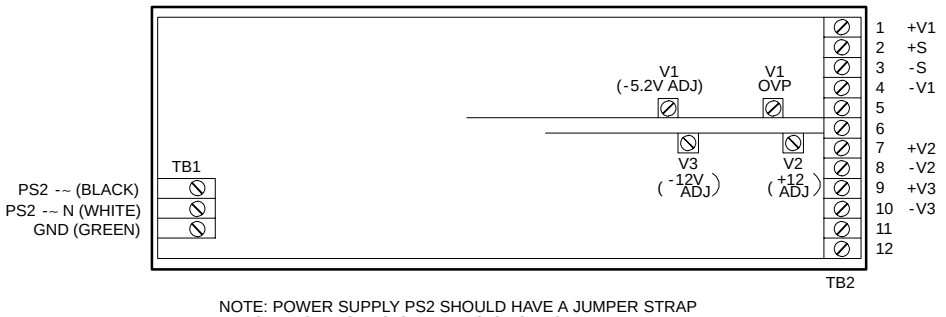
A5302



NOTE: POWER SUPPLY PS1 SHOULD HAVE A JUMPER STRAP FROM 3 TO 4.

Figure 5 - 1. Power Supply No. 1 Voltage Adjustments

A5303



NOTE: POWER SUPPLY PS2 SHOULD HAVE A JUMPER STRAP FROM TB2-1 TO TB2-2, AND TB2-3 TO TB2-4.

Figure 5 - 2. Power Supply No. 2 Voltage Adjustments

m. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

5–4 Fault Isolation (Troubleshooting)

Information to aid fault isolation within TM to an LRU is presented in table 5-3. This procedure is performed at the unit level with the TM LOCAL/CONTROL switch set to the LOCAL position. Before performing any procedures, refer to paragraph 3-5 for safety information. Procedures for troubleshooting the TM may be used in conjunction with troubleshooting procedures in the respective O&M manuals (see section 3, paragraph 3-11). If an LRU in the TM is faulty, refer to paragraph 5-7 for removal/replacement (R/R) procedures. The line maintenance technician (LMT) replaces the faulty LRU with a spare and sends the faulty assembly to the HMD for fault verification prior to shipment to the manufacturer for depot repair.

WARNING

Before attempting to perform any troubleshooting procedures, ensure that power has been removed (when possible) to prevent injury or DEATH from electric shock. It is recommended that at least two people are present at all times when working on energized equipment.

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

5–5 Preliminary Fault Isolation Steps

As a first step in fault isolation, perform the following preliminary steps. If any preliminary step leads to a possible fault, after correcting that possible fault, conduct paragraph 5-6 and verify that the fault(s) still exist.

a. Ensure all mechanical connections are secure. Check for improperly mated connectors, improperly seated PWAs, and evidence of physical damage.

b. Ensure power is available to unit.

c. Ensure (as nearly as possible) that all other equipment in, or associated with, the TM is operating properly.

d. Observe the front-panel display, indicators, and PWA LEDs for proper operation.

5–6 Operational Verification

This paragraph contains procedures that checkout and confirm the TM's Level 1 operational status while in local control. Before proceeding with any procedures involving the TM, refer to paragraph 3-5. Unless otherwise specified, all actions take place at the TM front panel. Upon any step which does not give a normal indication, stop operational verification procedure and proceed to table 5-3 and perform the fault isolation procedure.

a. Ensure paragraph 5-5, Preliminary Fault Isolation Steps has been completed in its entirety.

b. Place the ON/OFF switch to the OFF position.

c. Place the LOCAL/REMOTE switch to the LOCAL position.

d. Loosen the four captive screws holding the TM in the cabinet.

e. Slide the unit forward until the rail-guide locks are set to the locked position.

f. Using a flat-tipped screwdriver, loosen the four captive screws securing top cover to maintenance panel. Raise top cover to gain access to PWAs.

g. Place the ON/OFF switch to the ON position and verify the following:

(1) AC POWER indicator turns on.

Table 5 - 3. Fault Isolation			
STEP	PROCEDURE	EXPECTED RESULTS	FAULT ANALYSIS
1.	Ensure ON/OFF switch is in the OFF position and the LOCAL/ REMOTE switch is in the LOCAL position.	All front-panel indicators are turned off.	Faulty power switch
2.	Loosen the front panel screws, slide the TM forward until rail-guide locks are set to locked position.		
3.	Loosen top-cover screws and raise top cover to gain access to PWAs.	All PWA indicators are turned off.	
4.	Place the ON/OFF switch to the ON position.	The AC POWER indicator turns on. The cooling fan blowers turn on. The DC POWER indicators turn on.	Site-power not available CB101 faulty POWER ON indicator/ lampholder faulty Faulty fan Faulty indicator/lampholder Faulty power supply
5.	Using a digital multimeter, monitor dc power supply voltages at the maintenance panel.	See section 1, table 1 - 3.	Faulty power supply
6.	Using an oscilloscope, monitor the 1PPS EXT test point at the maintenance panel.	See section 1, table 1 - 3.	Site-supplied 1PPS signal not available
7.	Using a frequency counter, monitor the 10 MHZ test point at the maintenance panel.	See section 1, table 1 - 3.	Site-supplied 10-MHz signal not available

Table 5 - 3. Fault Isolation (Continued)

STEP	PROCEDURE	EXPECTED RESULTS	FAULT ANALYSIS
8.	Using an oscilloscope, monitor the 1PPS INT1 and INT2 at the maintenance panel.	Internally generated 1-Hz TTL signal with a 20% duty cycle.	SYNTH1 or 2 PWA faulty
9.	Press the RESET switch on maintenance panel.	The TEST indicator turns on and the NORMAL indicator turns off (except for 1-second test) for duration of the confidence BIT; the FAULT indicator remains turned off (except for 1-second test). At completion of the confidence BIT, the NORMAL indicator turns on and the TEST indicator turns off. The SELECT Menu is displayed.	Faulty indicator/lampholder View the MCP PWA and replace the MCP PWA if the RUN LED is turned on RED. If after replacing the MCP PWA, this fault continues to occur, systematically replace each PWA on the VMEbus until the PWA with the VME fault is found. Replace display or display power supply (PS3) if display remains blank and the MCP PWA RUN indicator is turned on GREEN. View the Confidence and Online BIT Results displays (figures 3 - 11 and 3 - 12) and replace faulty PWA/LRU identified.
10.	Select the Extended BIT Summary display (figure 3 - 7) and initiate the extended BIT processing. After all tests have completed, select Halt BIT and review LRU status	The TEST indicator turns on and the NORMAL indicator turns off for duration of the extended BIT; the FAULT indicator remains turned off. At completion of the extended BIT, the NORMAL indicator turns on and the TEST indicator turns off.	View the Extended BIT Results displays (figure 3 - 8 and 3 - 9) and replace faulty PWA/LRU identified by the display status View the MCP PWA and replace the MCP PWA if the RUN LED is turned on RED
11.	Perform Level 1 equipment group maintenance procedures to further isolate chassis fault.	Refer to applicable Level 1 O&M manual (see section 3, paragraph 3 - 8).	

Table 5 - 3. Fault Isolation (Continued)

STEP	PROCEDURE	EXPECTED RESULTS	FAULT ANALYSIS
12.	Replace chassis with good TM resident in STGT Electronics System Test Set (in the HMD area) if faulty LRU cannot be identified within Level 1 specified repair time.		

(2) Cooling fan blowers turn on.

(3) All seven DC POWER indicators turn-on.

(4) TEST indicator turns on

(5) All front-panel indicators turn on for a 1-second period.

(6) All STATUS indicators are turned off (after item 5 above).

h. Verify the TEST indicator turns off after approximately 10 seconds, the FAULT indicator remains turned off, and the NORMAL indicator turns on.

i. Verify the MCP PWA RUN LED is turned on green.

j. Verify the TM Select Menu (figure 3-5) appears on the display. If not, press previous menu until select menu appears.

k. Select maintenance and verify the Maintenance Menu (figure 3-6) appears.

l. Select confidence test results and verify the Confidence Test Results display (figure 3-11) appears.

m. Verify a status of GOOD appears for all confidence tested LRUs.

n. Select previous menu; at the Maintenance Menu select the display firmware version prompt.

o. Verify the Firmware Version display (figure 3-13) appears and the correct firmware versions are installed.

p. Select previous menu; at the Maintenance Menu select the display online BIT results.

q. Verify the Online BIT Results display (figure 3-12) appears and a status of “GOOD” appears next to all applicable online BIT tested LRUs.

r. Select previous menu; at the Maintenance Menu select Extended BIT Summary display.

s. Verify the Extended BIT Summary display (figure 3-7) appears; select Start BIT.

t. Select previous menu twice and verify the Select Menu appears.

u. At the Select Menu select configuration.

v. Verify the Configuration Menu (figure 3-16) appears.

w. At the Configuration Menu select Return Mod Service Config display.

x. Verify at the Return Mod Service Config display (figure 3-17) that the operation mode is extended BIT.

y. Select previous menu; at the Configuration display select Fwd Demod Service Config display.

z. Verify at the Fwd Demod Service Config display (figure 3-19) that the operation mode is extended BIT.

aa. Select previous menu twice and verify the Select Menu appears.

ab. At the Select Menu, select maintenance and verify the Maintenance Menu appears.

ac. At the Maintenance Menu select Extended BIT Summary display.

ad. Verify the Extended BIT Summary display (figure 3-7) appears; after a predetermined amount of time (enough time to ensure all extended BIT routines have been run; as shown on Extended BIT Summary display), select Halt BIT.

ae. Select Tests 1-8 and verify the display changes to BIT Results display (figure 3-8).

af. Verify all tests passed (view BIT Results screen 2 (figure 3-9) also; tests 9-12) and all applicable LRUs show a good status.

ag. Verify the MCP PWA RUN LED is turned on green.

ah. Verify the I488 PWA I488 FAIL LED is turned to green.

ai. Verify both SYNTH PWAs' LOCK LEDs are turned on.

aj. Select previous menu until the Select Menu appears.

ak. Verify the TEST indicator and the FAULT indicator are turned off and the NORMAL indicator is turned on.

al. Close top cover and using a flat-tipped screwdriver, tighten four top cover captive screws to maintenance panel.

am. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

an. Tighten four front-panel captive screws to the cabinet assembly.

ao. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

ap. Further TM operational verification is performed by utilizing the MTG. Refer to O&M manual applicable to suspect TM equipment group (see section 3, paragraph 3-11); otherwise, proceed with step aq.

aq. Place the REMOTE/LOCAL switch to the REMOTE position. Notify the TOCC2 operator that the TM is online and ADPE operation (remote control) is enabled.

5–7 Removal/Replacement

The following procedures provide removal and replacement instructions for TM major components. The procedures are presented in a step-by-step format to facilitate user comprehension and simplify task complexity. Tools or equipment required for removal and replacement of TM components are identified in the text, where applicable. These procedures assume that TM has been health tested in accordance with the procedures in paragraph 5-4 and that one or more LRUs have been identified as defective.

WARNING

Before attempting to perform any troubleshooting procedures, ensure that power has been removed (when possible) to prevent injury or DEATH from electric shock. It is recommended that at least two people are present at all times when working on energized equipment.

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

5–8 PWA Replacement

The TM PWAs are mounted in a card cage accessible from the top of the unit. The primary ac power must be turned off before replacing a PWA. When inserting PWAs, care must be used to ensure that connectors are properly aligned before applying engaging force. Perform the following procedure when a defective PWA is identified.

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Using a flat-tipped screwdriver, loosen four captive screws securing top cover to maintenance panel. Raise top cover to gain access to PWAs.

e. If needed, tag RF cable(s) connected to top of PWA to be replaced.

f. Disconnect RF cables from suspect PWA by gently pulling snap-on connector from PWA RF receptacle.

g. Using a flat-tipped screwdriver, loosen two captive screws securing PWA to chassis.

h. Grasping both PWA handles and pushing outwards, unseat and remove PWA.

NOTE

For the MCP PWA, SP7472500 - XXX IC chips (J21, J23, J25, and J27) and the DMDP PWA, SP7472110 - XXX IC chips (J11 and J12) must be removed from faulty PWA and inserted onto the new PWA. Perform the IC chip replacement paragraph; 5 - 9 prior to installing the new MCP or DMDP PWAs.

Figure 5 - 3 shows the MCP PWA jumper locations. Also shown are the four EPROM socket locations for SP7472500 - XXX IC chip set and proper installation alignment. Refer to table 5 - 4 for MCP PWA jumper descriptions/settings. Figure 5 - 4 shows the DMDP PWA EPROM socket locations for SP7472110 - XXX IC chip set and proper installation alignment. Figure 5 - 5 shows the I488 PWA jumper locations and settings.

i. Install replacement PWA in its appropriate slot and apply pressure to ensure proper seating.

j. Using a flat-tipped screwdriver, secure PWA to chassis with captive screws.

k. When applicable, reconnect tagged RF cables to replacement PWA by gently seating RF cable to PWA connector.

l. Inspect unit to ensure proper reassembly.

m. Close top cover and using a flat-tipped screwdriver, tighten four top cover captive screws to maintenance panel.

n. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

o. Tighten four front-panel captive screws to the cabinet assembly.

p. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

q. Perform paragraph 5-6 Operational Verification to verify TM operability.

5–9 IC Chip Replacement

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

a. Place faulty PWA on an ESD approved work bench.

b. For the MCP, refer to figure 5-3 and identify SP7472500-XXX IC chip set and chip key placement (J21, J23, J25, and J27). For the DMDP, refer to figure 5-4 and identify SP7472110-XXX IC chip set and chip key placement (J11 and J12).

c. Using a standard commercial IC chip puller, carefully extract IC chip set.

d. Place each chip in ESD approved conductive foam.

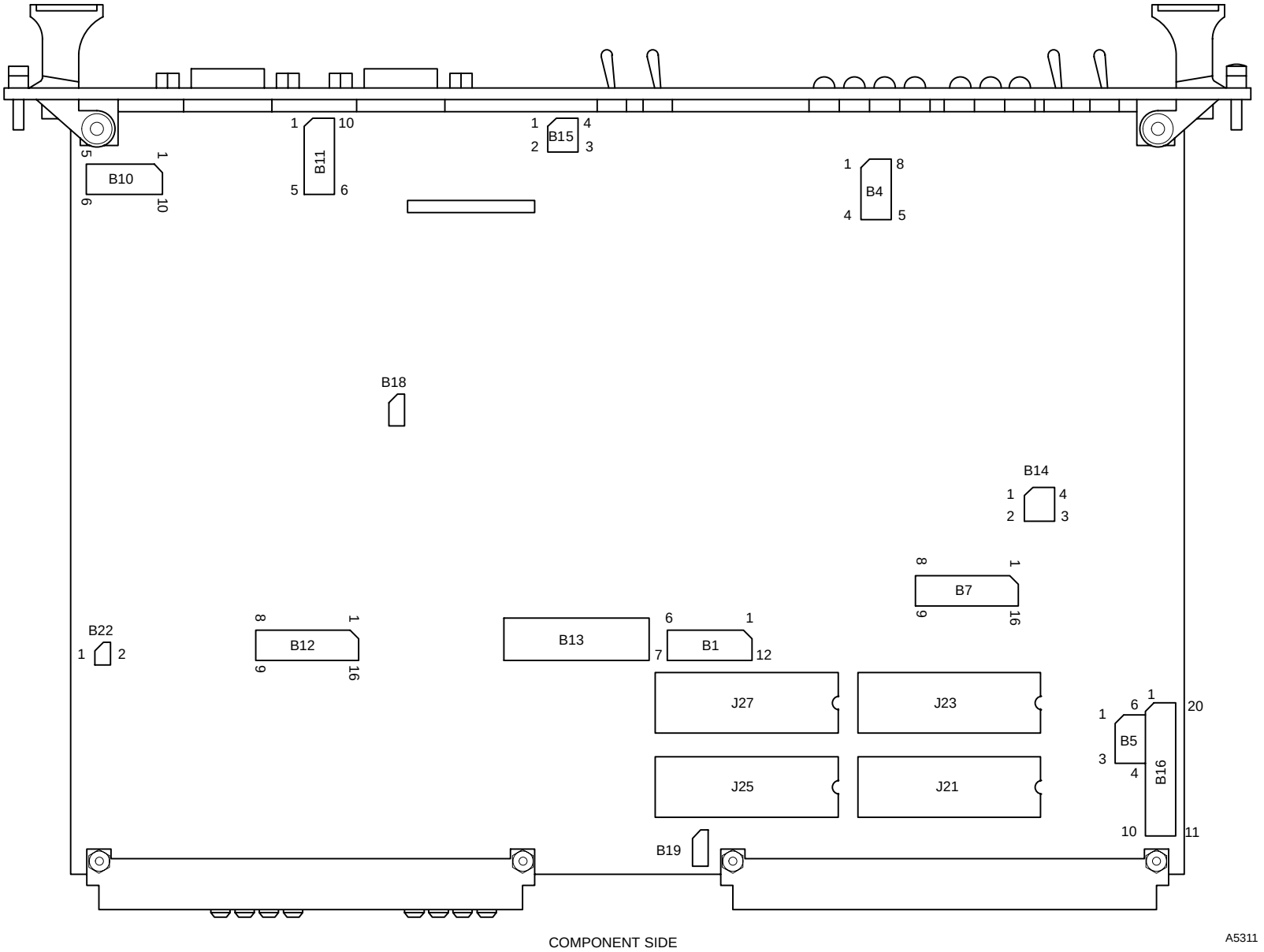


Figure 5 - 3. MCP PWA Component Location Diagram

Table 5 - 4. MCP PWA Jumper Configuration			
JUMPER BLOCK	JUMPER BLOCK JUMPER BLOCK DESCRIPTION	JUMPERS INSTALLED	CONFIGURED JUMPER FUNCTION
B1	Address comparator for SRAM	1 - 12, 3 - 10 5 - 6, 8 - 9	1 Mbyte local SRAM
B4	Access time selection for EPROM area	3 - 6, 4 - 5	200 ns EPROMS
B5	Clock to bus Reset to bus Reset from bus	1 - 6, 2 - 5, 3 - 4	Clock enabled to bus Reset enabled to bus Reset enabled from bus
B7	EPROM area address decoding	1 - 16, 2 - 15, 3 - 14, 4 - 13	EPROM type: 27C010 Organization: 512K x 8
B10	Serial interface MPCC1 RS232 control	2 - 3, 4 - 7, 5 - 6	DSR - DSR (OUT) DCD - CTS (IN) DTR - DTR (OUT)
B11	Serial interface MPCC2 RS232 control RS422/485 control	2 - 3, 4 - 7, 5 - 6	- DSR - CTS - DTR
B12	VME bus interrupts	1 - 16, 2 - 15, 3 - 14, 4 - 13, 5 - 12, 6 - 11, 8 - 9	IRQ1 thru IRQ6 enabled IRQ7 disabled VME PROM disabled
B13	User I/O, S/W readable	None	Not used
B14	Long time bus error enable	2 - 3	4.65 to 4.70 volt threshold
B15	Threshold of the power voltage detector	1 - 4	
B16	Serial interface MPCC2 RS232 control RS422/485 control	1 - 20, 3 - 18, 4 - 17, 5 - 6, 7 - 14, 11 - 12 15 - 16	Bus request level 3
B18	Abort to IRQ7	None	Not used
B19	Power standby for the SRAM 4.5V min.	None	Standby power disabled
B22	VSB enable/disable	1 - 2	VSB disabled

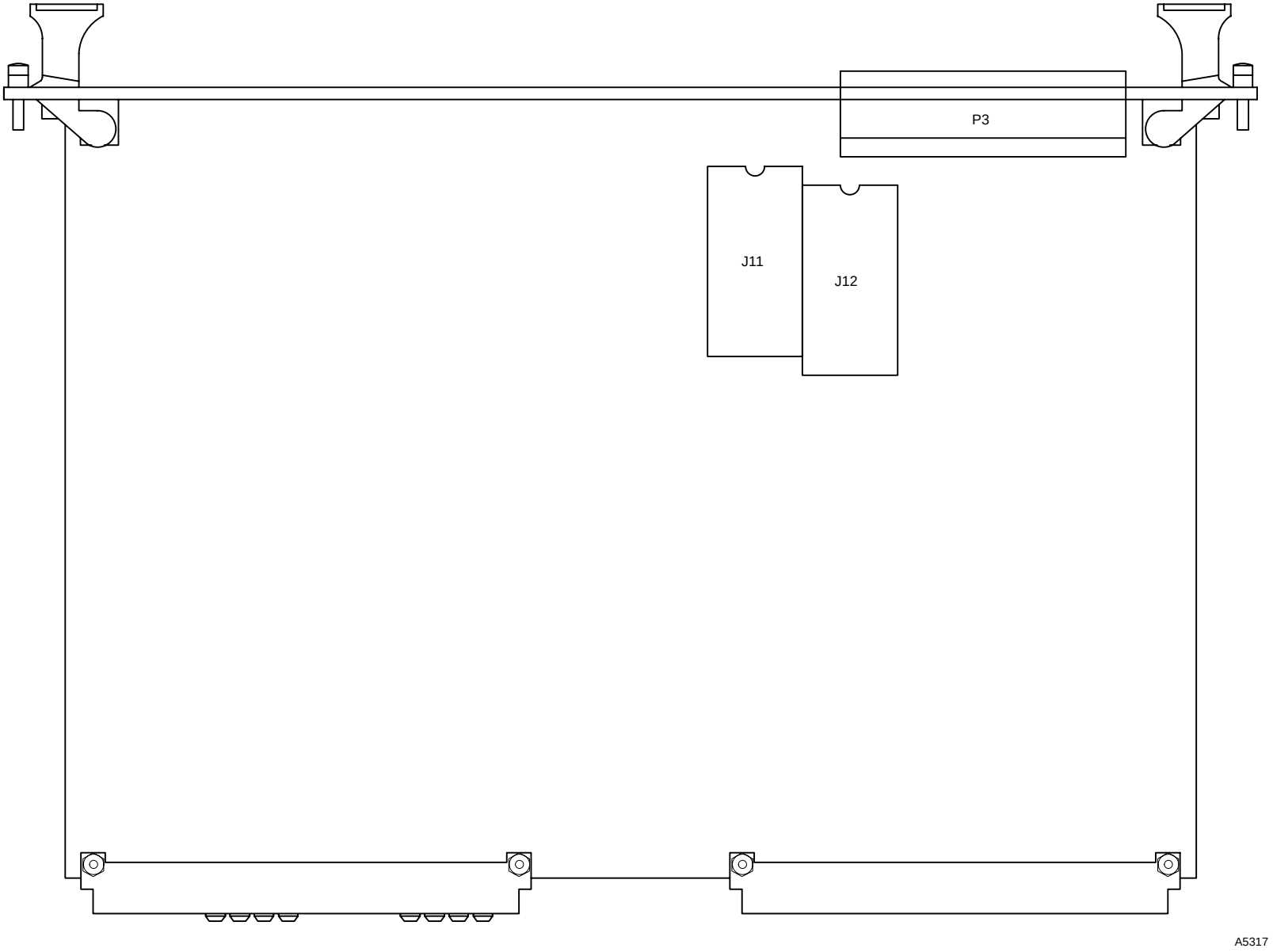
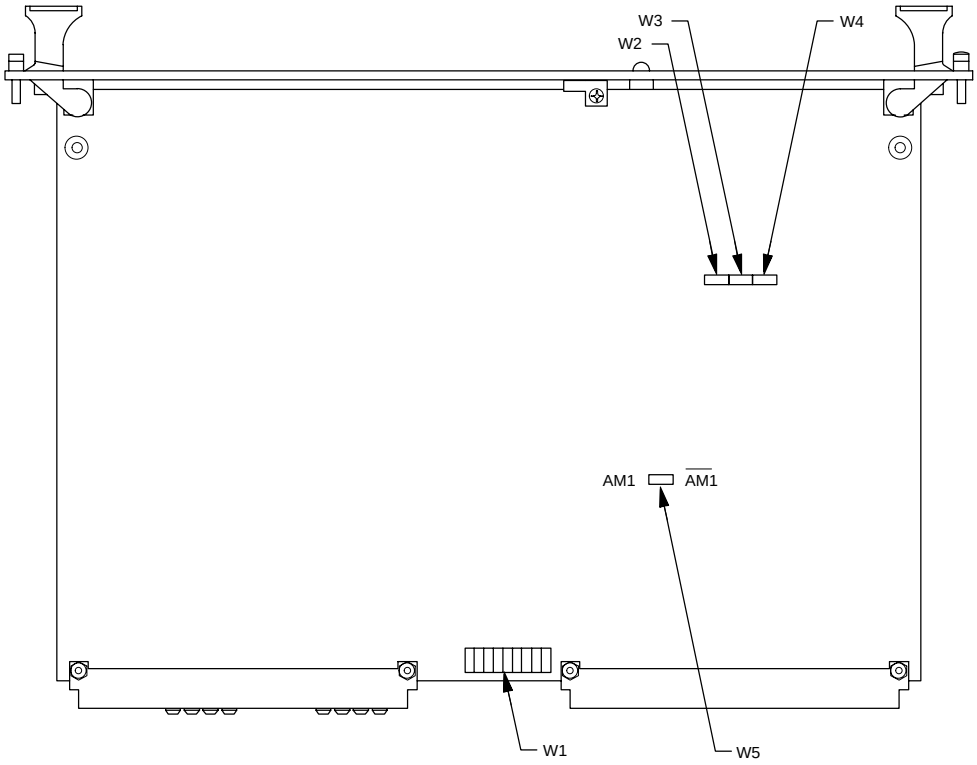


Figure 5 - 4. DMDP PWA Component Location Diagram



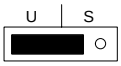
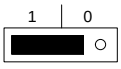
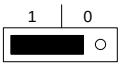
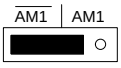
JUMPER CONFIGURATION CHART			
JUMPER BLOCK	JUMPER BLOCK DESCRIPTION	JUMPERS INSTALLED	CONFIGURED JUMPER FUNCTION
W1	BOARD BASE ADDRESS (SHORT I/O ADDRESS)		BASE ADDRESS: $FCFF0000
W2	INITIAL ACCESS MODE AFTER RESET		USER MODE, RESPONSE TO AM CODE $29
W3	ADDRESS MODIFIER AM5		AM5 = 1 (AM CODE $39)
W4	ADDRESS MODIFIER AM3		AM3 = 1 (AM CODE = $39)
W5	ADDRESS MODIFIER AM0		AM0 = AM1 $\overline{\text{(AM CODE = \$39)}}$

Figure 5 - 5. I488 PWA Jumper Location/Settings Diagram

e. Package faulty PWA as per procedure in section 2; paragraph 2-7.

f. Place new PWA on ESD approved work bench.

g. Referring to applicable figure (5-3 or 5-4) re-insert IC chip set. Ensure chip key placement is correct.

h. Referring to figure 5-3 and table 5-4, verify/ ensure all MCP PWA jumper settings are correct.

i. Replace PWA per procedure in paragraph 5-8.

5–10 Cooling Fan Replacement

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Disconnect ac power cord from rear panel connector J101.

e. Using a flat-tipped screwdriver, loosen four captive and eight quick-disconnect screws securing top cover and remove top cover.

f. Remove air filter at rear of unit by sliding filter upward.

g. Disconnect/tag ac power plug from suspect fan.

h. Using a flat-tipped screwdriver, remove four each flat-head screws, flat washers, and lock nuts retaining faulty fan.

i. Remove faulty fan and protective cover.

j. Mount replacement fan and previously removed protective cover by replacing four each flat-head screws, flat washers, and lock washers previously removed in step (h).

k. Reconnect air filter ac power plug and air filter.

l. Replace top cover and using a flat-tipped screwdriver, tighten four captive screws to maintenance panel and eight quick-disconnect screws to chassis.

m. Reconnect ac power cord to rear panel connector J101.

n. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

o. Tighten four front-panel captive screws to the cabinet assembly.

p. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

q. Perform paragraph 5-6 Operational Verification to verify TM operability.

5–11 PS1 and PS2 Replacement

NOTE

Before replacing suspect faulty power supply, attempt to correct power supply fault by toggling unit power to reset power supply circuit breaker and then perform the adjustment procedures in paragraph 5 - 3.

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Disconnect ac power cord from rear panel connector J101.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

e. Applying pressure to bottom cover towards unit chassis, use a flat-tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

f. Carefully lower bottom panel to gain access to power supplies.

g. Tag all power lines connected to suspect power supply.

h. Disconnect power lines from power supply terminals using a flat-tipped screwdriver.

CAUTION

Secure power supply by applying pressure/firmly holding as mounting screws are removed. Failure to do so may result in damage to power supply due to slippage.

i. While applying pressure to power supply, use a No. 2 cross-tipped screwdriver to remove (four - PS2 or three - PS1) pan-head locking screws securing suspect power supply to bottom cover and store power supply in a secure area.

j. While firmly holding new power supply, use No. 2 cross-tipped screwdriver to replace (four - PS2 or three - PS1) pan-head locking screws removed in step (i) to secure power supply to bottom cover.

k. Reconnect power lines to their appropriate terminals using a flat-tipped screwdriver.

l. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

m. Reconnect ac power cord to rear panel connector J101.

n. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

o. Tighten four front-panel captive screws to the cabinet assembly.

p. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

q. Perform paragraph 5-3 before operating TM.

r. Perform paragraph 5-6 Operational Verification to verify TM operability.

5–12 PS3 Replacement

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Disconnect ac power cord from rear panel connector J101.

e. Using a flat-tipped screwdriver, loosen four captive screws securing top cover to maintenance panel and raise top cover.

f. Disconnect connector P6 from the maintenance panel connector J6.

g. Using a No. 2 cross-tipped screwdriver, remove four pan-head screws securing maintenance panel to unit chassis.

h. Carefully lift maintenance panel and tag/disconnect RF cables from maintenance panel connectors J1 through J5. Carefully store maintenance panel in a secure area.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

i. Applying pressure to bottom cover towards unit chassis, use a flat-tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

j. Carefully lower bottom panel to gain access to terminal board 2 (TB2).

k. Using a flat-tipped screwdriver, disconnect the three ac power lines and 130 vdc lines (log which wires attach to which TB2 terminals) from TB2 terminals which originate from PS3. Remove S1 and TB2.

l. Using a No. 2 cross-tipped screwdriver, remove four flat-head screws securing power supply cover to chassis side panel and carefully store it in a secure area.

CAUTION

Secure power supply No. 3 by applying pressure/firmly holding as mounting screws are removed. Failure to do so may result in damage to power supply due to slippage.

m. While applying pressure to power supply, use a No. 2 cross-tipped screwdriver to remove two flat-head screws securing PS3 bracket to chassis side panel.

n. Remove PS3 from unit and at workbench, remove bracket assembly from defective PS3 and attach to new PS3. Store defective PS3 in a secure area.

o. While firmly holding new PS3 with bracket, use No. 2 cross-tipped screwdriver to replace two flat-head screws removed in step (m) to secure power supply to chassis side panel.

p. Reposition power supply cover over PS3 with power lines fed through feed-hole.

q. Using a No. 2 cross-tipped screwdriver, replace four flat-head screws securing power supply cover to chassis side panel.

r. Using a flat-tipped screwdriver, reconnect the three ac power lines and 130 vdc lines to TB2 terminals (refer to log taken in step k).

s. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

t. Carefully lift maintenance panel and reconnect previously tagged RF cables to maintenance panel connectors J1 through J5.

u. Carefully place maintenance panel into its correct position within the chassis and using a No. 2 cross-tipped screwdriver, replace the four pan-head screws securing the maintenance panel to the chassis.

v. Reconnect connector P6 to the maintenance panel connector J6.

w. Inspect TM to ensure proper reassembly.

x. Close top cover and using a flat-tipped screwdriver, tighten four top cover captive screws to maintenance panel.

y. Reconnect ac power cord to rear panel connector J101.

z. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

aa. Tighten four front-panel captive screws to the cabinet assembly.

ab. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

ac. Perform paragraph 5-6 Operational Verification to verify TM operability.

5–13 Touch Panel Display Replacement

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Disconnect ac power cord from rear panel connector J101.

e. Using a flat-tipped screwdriver, loosen four captive screws securing top cover to maintenance panel and raise top cover.

f. Disconnect connector P6 from the maintenance panel connector J6.

g. Using a No. 2 cross-tipped screwdriver, remove four pan-head screws securing maintenance panel to unit chassis.

h. Carefully lift maintenance panel and lay against card cage.

i. Using a No. 2 cross-tipped screwdriver, remove four pan-head screws securing touch panel screen. Carefully remove screen assembly by prying assembly loose from guide pins on front panel assembly. Store screen assembly in a secure area.

CAUTION

Secure display panel by applying pressure/firmly holding as screws and connectors are removed. Failure to do so may result in damage to panel due to slippage.

j. While applying pressure to display panel, use a No. 2 cross-tipped screwdriver to remove four outer flat-head screws securing panel to unit front panel.

k. While firmly holding display panel, remove connectors (A7P3 and A7P4) to release panel from unit front panel.

l. While firmly holding display panel, use No. 2 cross-tipped screwdriver to remove four flat-head screws holding panel in its housing and remove panel from housing. Place defective display panel in a secure area.

NOTE

The infrared emitters and sensors associated with the display panel switch function are mounted on the electronic module. They fire toward the display viewer and depend upon prisms mounted along the bezel periphery to reflect the infrared beams parallel to the display surface. This scheme requires careful attention to display panel mounting. The under surface of the bezel must be held parallel to the top of each of the four spacers upon which the electronic module mounts to the rear of the unit front panel.

Prior to installing display panel to unit front panel, ensure that DIP switches 1, 2, and 3 located on the display control boards are set properly for the unit configuration (refer to figure 5 - 6). Compare with replaced display panel to ensure proper switch settings.

m. Install new display panel in housing.

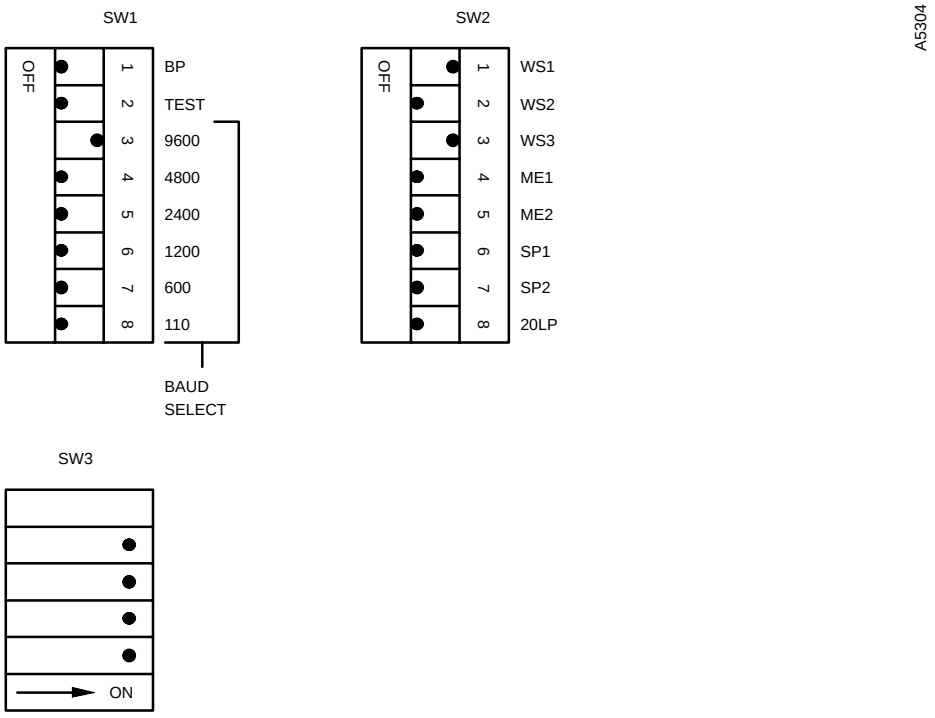


Figure 5 - 6. Touch Panel Display Dip Switch Settings

n. While firmly holding display panel, use No. 2 cross-tipped screwdriver to replace four flat-head screws removed in step (l) to secure panel to housing (two longer screws go in top two positions).

CAUTION

Secure display panel by applying pressure/firmly holding as screws and connectors are replaced. Failure to do so may result in damage to panel due to slippage.

o. While firmly holding display panel, replace connectors removed in step (k).

p. While applying pressure to display panel, secure panel to unit by using a No. 2 cross-tipped screwdriver to replace four flat-head screws removed in step (j).

q. Reinstall the block touch panel screen by using a No. 2 cross-tipped screwdriver to replace the four pan-head screws removed in step (i).

r. Carefully lift maintenance panel and reconnect previously tagged RF cables to maintenance panel connectors J1 through J5.

s. Carefully place maintenance panel into its correct position within the chassis and using a No. 2 cross-tipped screwdriver, replace the four pan-head screws securing the maintenance panel to the chassis.

t. Reconnect connector P6 to the maintenance panel connector J6.

u. Inspect TM to ensure proper reassembly.

v. Close top cover and using a flat-tipped screwdriver, tighten four top cover captive screws to maintenance panel.

w. Reconnect ac power cord to rear panel connector J101.

x. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

y. Tighten four front-panel captive screws to the cabinet assembly.

z. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

aa. Perform paragraph 5 - 6 Operational Verification to verify TM operability.

5–14 Lamp Replacement

a. Grasp the lamp cover with the thumb and forefinger and remove it by unscrewing it from the lampholder assembly.

b. Grasp the lamp with the thumb and forefinger and remove it by pulling outward.

c. Reinsert replacement lamp; lamp is keyed so it will fit into lampholder only one way.

d. Replace lamp cover by screwing it back onto the lampholder; do not overtighten.

e. Verify proper operation of replacement lamp by running the confidence BIT.

f. Perform paragraph 5 - 6 Operational Verification to verify TM operability.

5–15 Lampholder Replacement

a. Preheat a soldering iron.

b. Set AC POWER ON/OFF switch to OFF.

c. Loosen the four captive screws holding the unit in the cabinet.

d. Slide the unit forward until the rail guide locks are set to the locked position.

e. Disconnect ac power cord from rear panel connector J101.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

f. Applying pressure to bottom cover towards unit chassis, use a flat-tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

g. Carefully lower bottom panel to gain access to suspect lampholder.

h. Remove protective heat shrink from lampholder connectors. Wrap may be removed by slipping it down the wire or by carefully cutting it off using a pair of snub-nosed wire cutters or x-acto knife.

i. Tag lampholder wires connected to positive and negative leads.

j. Using preheated soldering iron, unsolder tagged wire connected to lampholder leads.

k. Using 1/2” open-end wrench, grasp mounting flange nut (on inside of front panel) holding lampholder to chassis. With free hand, grasp lampholder section on outside of front panel.

l. Unscrew flange nut and remove lampholder from chassis.

m. Replace new lampholder into front panel and screw flange nut finger tight onto chassis.

n. Using 1/2” open-end wrench, grasp mounting flange nut (on inside of front panel) holding lampholder to chassis. With free hand, grasp lampholder section on outside of front panel.

o. Tighten flange nut to ensure a firm mounting to chassis.

p. Place or ensure that an ample amount of heat shrink is resident on each wire prior to soldering.

q. Using the preheated soldering iron, solder previously removed wires to respective positive and negative lampholder leads.

r. Shift the heat shrink so it covers the new soldered joint.

s. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

t. Reconnect ac power cord to rear panel connector J101.

u. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

v. Tighten four front-panel captive screws to the cabinet assembly.

w. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

x. Perform paragraph 5-6 Operational Verification to verify TM operability.

5–16 Switches and Circuit Breaker Replacement

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Disconnect ac power cord from rear panel connector J101.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

e. Applying pressure to bottom cover towards unit chassis, use a flat-tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

f. Carefully lower bottom panel to gain access to switches and circuit breaker.

g. Tag all wires connected to suspect switch or circuit breaker after removing heat shrink that surrounds switch or circuit breaker with x-acto knife.

h. Using the appropriate flat-tipped or cross-tipped screwdriver, disconnect wire leads connected to suspect switch or circuit breaker.

i. Using 9/16” open-end wrench, grasp mounting flange nut (on outside of panel) holding suspect switch or circuit breaker to chassis. With free hand, grasp section on inside of panel.

j. Unscrew flange nut and remove from chassis.

k. Replace new switch or circuit breaker into panel and screw flange nut finger tight onto chassis.

l. Using 9/16” open-end wrench, grasp mounting flange nut (on outside of panel) holding switch or circuit breaker to chassis. With free hand, grasp section on inside of panel.

m. Tighten flange nut to ensure a firm mounting to chassis.

n. Place ample amount of heat shrink on switch.

o. Using appropriate flat-tipped or cross-tipped screwdriver, re-connect wire leads to new switch or circuit breaker.

p. Using a heat blower gun, form heat shrink over switch to adequately cover power leads.

q. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

r. Reconnect ac power cord to rear panel connector J101.

s. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

t. Tighten four front-panel captive screws to the cabinet assembly.

u. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

v. Perform paragraph 5-6 Operational Verification to verify TM operability.

5–17 Preventive Maintenance

Preventive maintenance serves to keep the equipment in proper operating condition, to prevent breakdown, and to hold needless repair to a minimum. This information includes cleaning equipment required and instructions for preventive maintenance. As a general rule, the preventive maintenance measures detailed in the following paragraphs should be accomplished once a month or per site requirements. When the unit is operated under severe contamination conditions (for example, dust or dirt) a shorter preventive maintenance interval is recommended. Turn off or disconnect the input power before performing the preventive maintenance procedures.

WARNING

Before attempting to perform inspection or preventive maintenance, ensure that power has been removed to prevent injury or DEATH from electric shock.

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

5–18 Inspection

Visual inspection of the unit should be performed once every 30 days or per site requirements. Visually inspect the unit to determine if the item is damaged or incomplete to the extent that it should be repaired or replaced. Perform the visual inspection procedures in table 5-5.

5–19 Preventive Maintenance Steps

Preventive maintenance consists of inspection, cleaning, and voltage checks. The unit should be cleaned every 30 days or per site requirements. Clean exterior surfaces using a clean lint-free cloth to remove dust or grease. Perform interior preventive maintenance as follows:

Table 5 - 5. Inspection and Maintenance Criteria			
ITEM	NOMENCLATURE	INSPECT FOR	REPAIR
1	Exterior	Dents, scratches, loose cable connectors, paint damage	Repair or replace
2	Interior	Dents, scratches, loose cable connectors, broken wires, evidence of burned or charred components, defective solder connections	Repair or replace

a. Using a vacuum cleaner, remove loose dust and dirt from card cage, PWAs, and interior surface.

b. Use a soft-bristle brush to remove dirt that adheres to the card cage, PWAs, and interior surfaces.

c. Remove air filter from behind 3-form frame, clean using a vacuum cleaner or reverse flushing with water, and replace air filter when dry.

d. Verify fan (3) rotation is free of restriction. Clean fan blades of dust accumulation.

e. Using a digital voltmeter, verify power supply voltages (via the maintenance panel test points) are within specification. Refer to paragraph 5-3 if adjustments are necessary.

Section 6 — Parts List

6–1 Introduction

This section lists, describes, and illustrates a breakdown of items necessary to support the Test Modem. The purpose of the breakdown is to assist supply and maintenance personnel in identifying, requesting, and stockpiling TM replacement parts.

6–2 List of Manufacturers

Table 6-2 contains the list of manufacturer commercial and government entity (CAGE) numbers/federal supply code for manufacturers (FSCM), names, and addresses for all items listed in the parts lists.

6–3 Maintenance Parts List

The maintenance parts lists (MPLs) (refer to table 6-1 for a list of MPLs, tables 6-3 through 6-6) provide a description of each major assembly, subassembly, and attaching part listed, keyed to the applicable figure (e.g., figure 6-2, index 4 is identified in the first column of the corresponding MPL as 6-2-4). Other information in the MPLs include item reference designator, item nomenclature/description, manufacturer's code (CAGE/FSCM), item part number, and number of units per assembly. These items are all described in the following paragraphs.

6–4 Reference Designator Column

The reference designator allows for an indexed item designation reference to the top assembly.

6–5 Figure and Index Number Column

This column lists the applicable index numbers called out on the associated figure.

6–6 Description Column

This column contains the nomenclature and description of each assembly, subassembly, or attaching part. Subassemblies within an assembly are indented under that assembly with individual index numbers assigned to them. Attaching parts hardware is indented under the item it attaches, and the description is followed by the attaching part annotation "(AP)."

6–7 Cage/FSCM Column

This column provides the parts manufacturers' CAGE/FSCM codes. These codes relate to the manufacturers listed in table 6-2 and are in accordance with Federal Supply Codes for Manufacturers Cataloging books H4-1, H4-2, and H4-3.

6–8 Part Number Column

This column contains the manufacturer's part number for the indexed part in the associated figure. A number sign (#) following the part number indicates that the item is either government-furnished equipment (GFE), contractor-furnished equipment (CFE), or attachment hardware covered in other manuals.

6—9 Quantity Column

This column indicates the quantity required for an assembly, subassembly, or piece part. If quantities are indefinite (i.e., adhesive, locktite, etc.), an “AR” is placed in this column to indicate “as required.” If the quantity of the item has been called out in a previous figure or if the item must be removed to gain access to a spared item, a “REF” is placed in this column to indicate “reference”.

6—10 Illustrations

Figures 6-1 through 6-4(refer to table 6-1 for a list of parts illustrations) are illustrated parts breakdowns (IPBs) showing the major assemblies, subassemblies, and attaching parts associated with the TM. Individual items in each figure are identified with an index number and keyed to the corresponding MPL, which normally faces and immediately follows the figure.

Table 6—1. List of Parts Lists and Figures

Table 6—2. Index to Manufacturers CAGE/FSCM Numbers		
CAGE/ FSCM	MANUFACTURER	ADDRESS
03102	Supreme Supply Co.	734 E. Hyde Park Blvd. P.O. Box 922 Inglewood, CA 90302—2508
05236	Jonathan Mfg. Co.	Fullerton, CA
07421	Interstate Electronics Corp.	1001 E. Ball Road P.O. Box 3117 Anaheim, CA 92803
08742	Emerson Electric Co.	ACDC Electrics Div. 401 Jones Rd. Oceanside, CA 92054—1216
09353	C and K Components Inc.	15 Riverdale Ave. Newton, MA 02158—1057
25140	Globe Motors	2275 Stanley Ave. Dayton, Ohio 45404
27193	Eaton Corp.	Aerospace/Commercial Controls Div. Milwaukee, WI
28979	Loral Corp/Microware Wavecom Division	Northridge, CA
72619	Dialight Corp.	Brooklyn Div. 203 Harrison Pl. Brooklyn, New York 11237—1587
80205	National Aerospace Standards Committee Aerospace Industries Association of America, Washington, DC. Sources of supply for all of the National Aerospace Standards have been identified and compiled into a reference book published by the National Standards Association. This book is available through Federal Supply Schedule 76, Part I.	
80103	VEECO Instruments Inc.	Lambda Electronics Div. 515 Broad Hollow Rd. Melville, New York 11747—3703
81349	Military specifications promulgated by military departments/agencies under authority of Defense Standardization Manual 4120 3—M.	
8Z410	Ledtronics Inc.	Harbor City, CA
96906	Military specifications promulgated by military departments/agencies under authority of Defense Standardization Manual 4120 3—M.	
NMB	NMB Technologies Inc.	Motor Division Chatsworth, CA

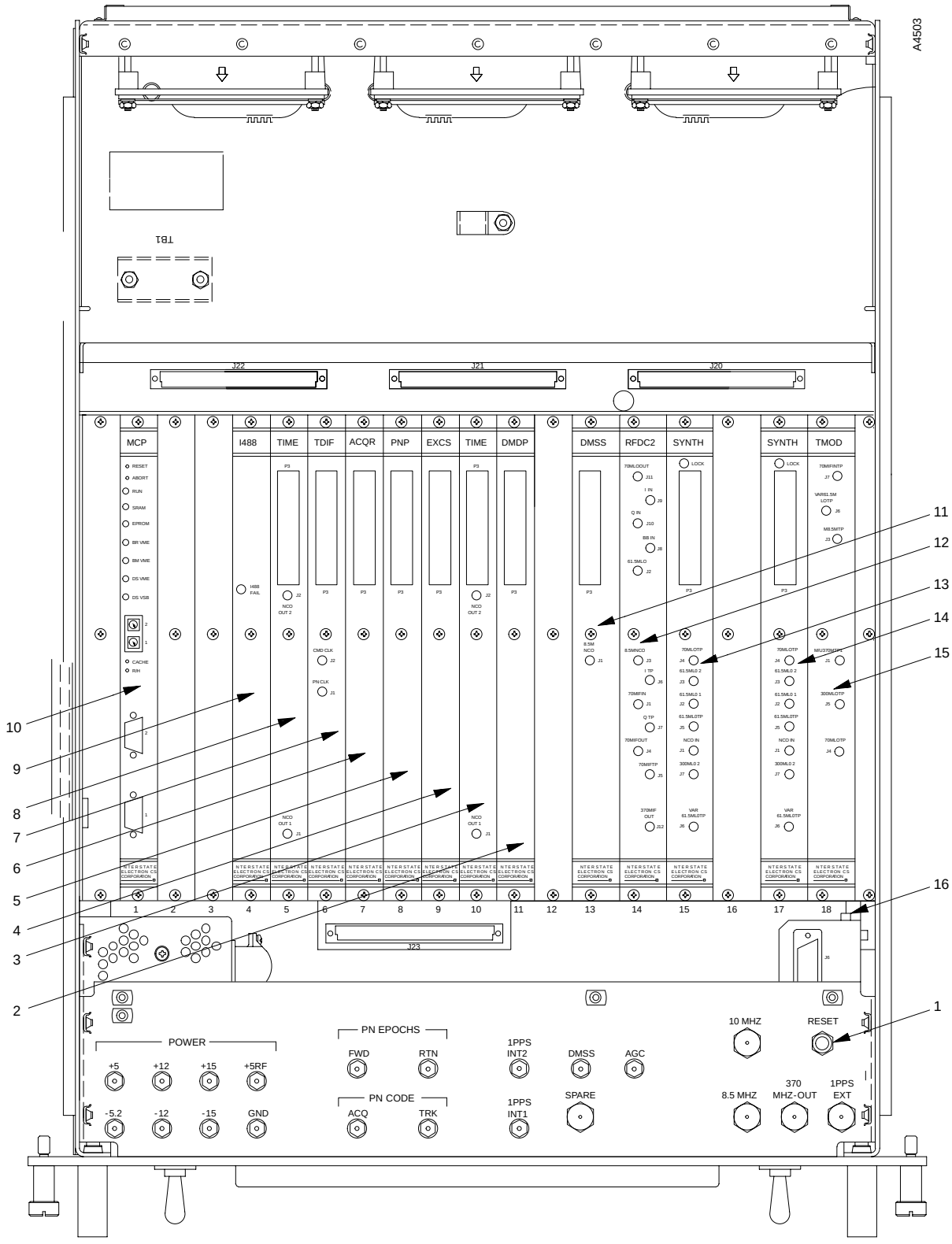


Figure 6—1. Test Modem (Top View)

Table 6—3. Parts List, Test Modem (Top View)

REF. DES.	FIGURE/ IND. NO.	DESCRIPTION	CAGE/ FSCM	PART NUMBER	QTY
1	6-1	Test Modem (Top View)	07421	7472500	REF
1A6SW4	6-1-1	. Switch, Push . . Cap, Nylon (AP)	09353 09353	8121ZE 7527-2	1 1
A4A11	6-1-2	. Demod Processor PWA . . Firmware Chip Set (J11 and J12) (AP)	07421 07421	7476100 SP7472110-XXX *	1 1
1A4A10, 1A4A5	6-1-3, 6-1-8	. Timing Generator PWA	07421	7473000-502	2
1A4A9	6-1-4	. External Clock Synchronizer PWA	07421	7510400-501	1
1A4A8	6-1-5	. PN Processor PWA	07421	7473300-501	1
1A4A7	6-1-6	. Acquistion Processor PWA	07421	7473200-501	1
1A4A6	6-1-7	. Test Data Interface PWA	07421	7473900-501	1
1A4A4	6-1-9	. 488 Interface Control PWA	07421	7473700	1
1A4A1	6-1-10	. Modem Control Processor PWA . . Firmware Chip Set (J21, J23, J25, and J27) (AP)	07421 07421	7473600 SP7472500-XXX *	1 1
1A4A13	6-1-11	. Demodulator Symbol Synchronizer PWA 1	07421	7473100-502	1
A4A14	6-1-12	. RF Downconverter No. 2 PWA	07421	7474300-500	1
1A4A15, 1A4A17	6-1-13, 6-1-14	. Synthesizer PWA	07421	7474600-500	2
1A4A18	6-1-15	. Test Modulator PWA	07421	7475000-500	1
1A6SW3	6-1-16	. Switch, RF Coaxial	28979	8021-A35 A4B-1C0	1

NOTES: *(XXX) represents the current firmware version.
Refer to figures 5-3 and 5-4 for chip location/placement.

A4498

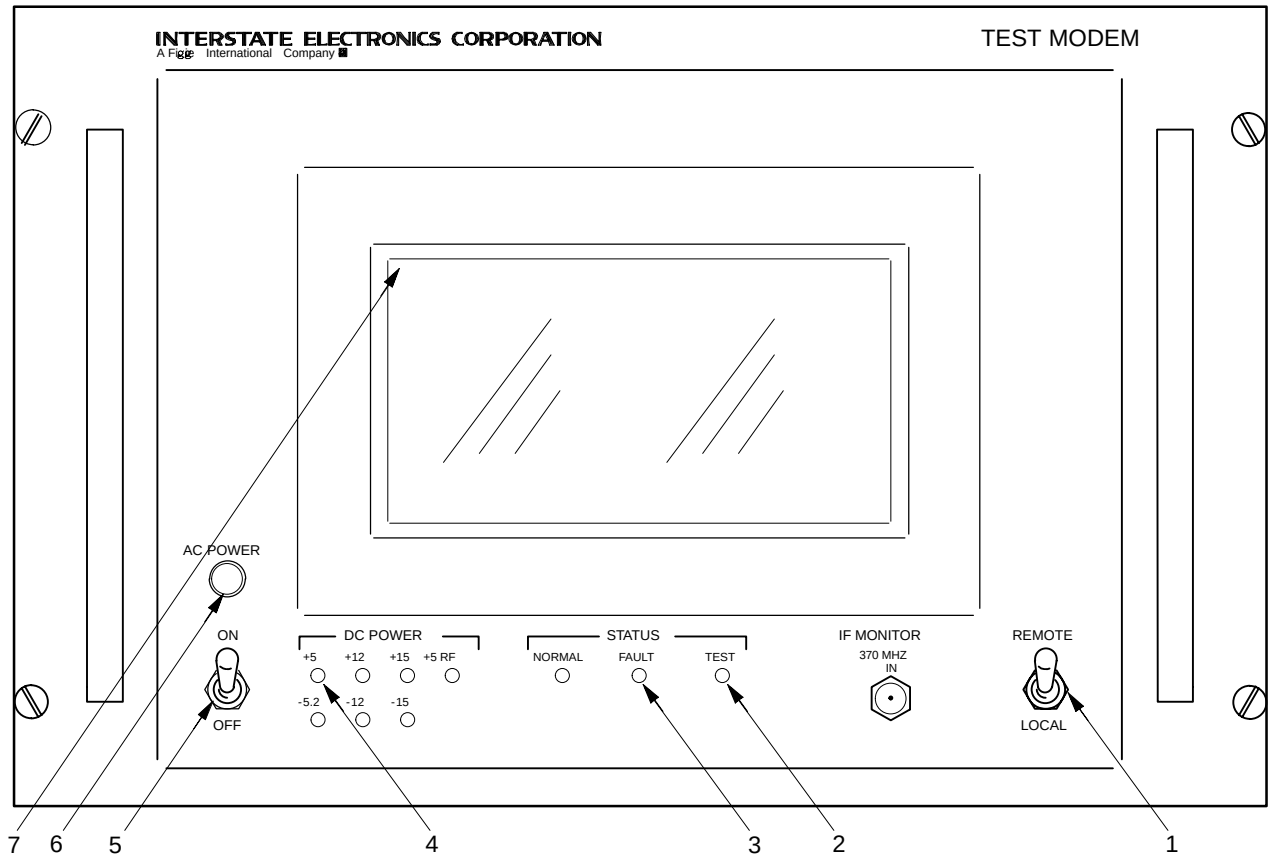


Figure 6—2. Test Modem (Front View)

Table 6—4. Parts List, Test Modem (Front View)					
REF. DES.	FIGURE/ IND. NO.	DESCRIPTION	CAGE/ FSCM	PART NUMBER	QTY
1	6—2	Test Modem (Front View)	07421	7472500	REF
1A7SW2	6—2—1	. Switch, Toggle	96906	MS24658—23F	1
1A7DS8	6—2—2	. Lamp, Cartridge . . Lampholder	72619 8Z410	507—4957—3733—500 DH0—30Y—D86BWC	1 1
1A7DS7	6—2—3	. Lamp, Cartridge . . Lampholder	72619 8Z410	507—4757—3731—500 DH0—30Y—D86BWC	1 1
1A7DS2—DS6,DS9—DS11	6—2—4	. Lamp, Cartridge . . Lampholder	72619 8Z410	507—4857—3732—500 DH0—30Y—D86BWC	8 8
1A7SW1	6—2—5	. Switch	81349	MS24659—22F	1
1A7DS1	6—2—6	. Lamp (LED), Cartridge	8Z410	CF296CWPG6—120VAC—R	1
1A7A1	6—2—7	. Touch Panel Display	07421	7519500	1

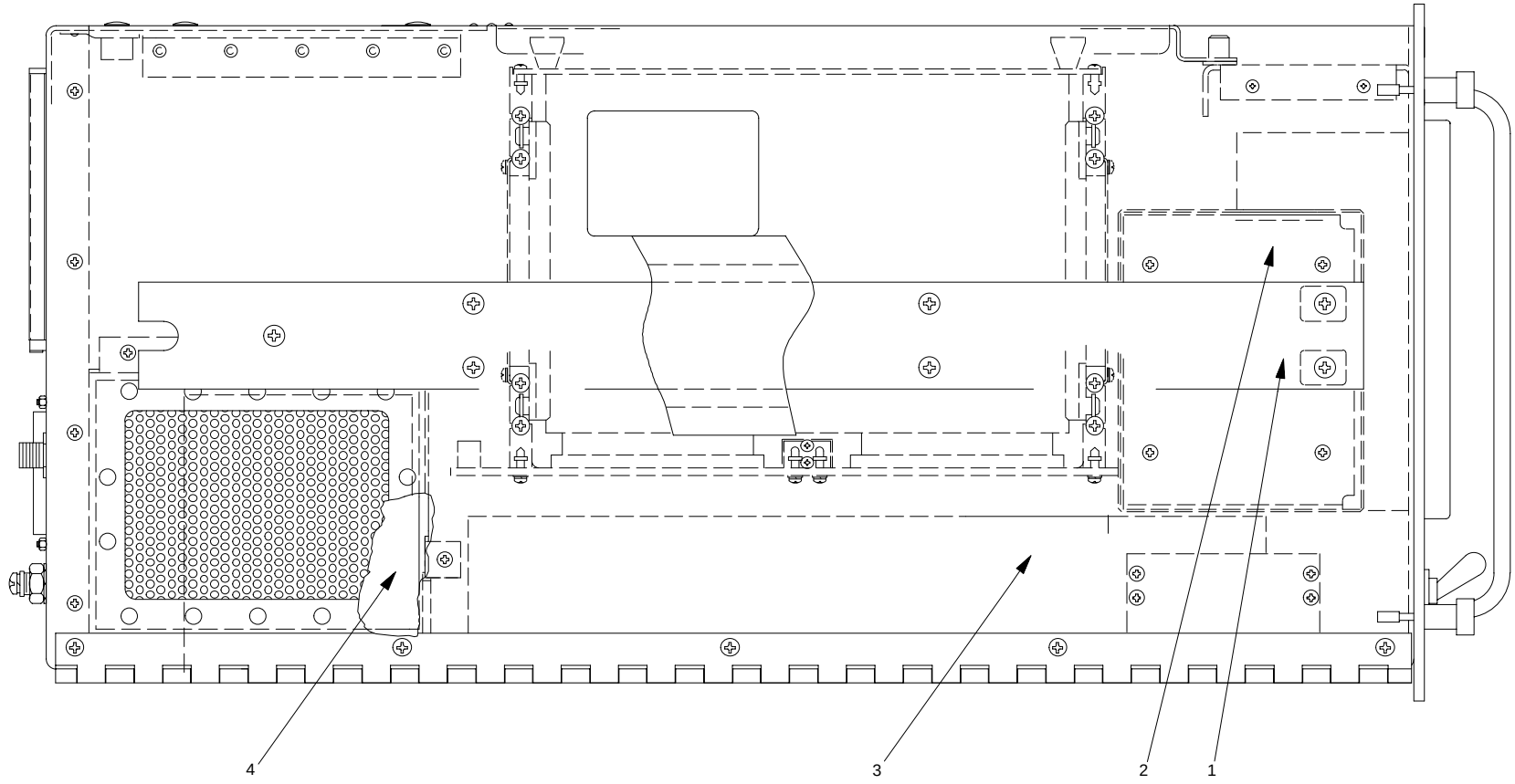


Figure 6–3. Test Modem (Side View)

A4266

Table 6—5. Parts List, Test Modem (Side View)					
REF. DES.	FIGURE/ IND. NO.	DESCRIPTION	CAGE/ FSCM	PART NUMBER	QTY
1	6—3	Test Modem (Side View)	07421	7472500	REF
	6—3—1 (Not Shown)	. Slide, Section (Left)	05236	1505772B—L	1
		. . Screw, Cres FLH100 10—32X5/8 (AP)	96906	MS24693—C273	7
	6—3—1	. Slide, Section (Right)	05236	1505772B—R	1
		. . Screw, Cres FLH100 10—32X5/8 (AP)	96906	MS24693—C273	7
1A5	6—3—2	. Power Supply No. 3	07421	7516900	1
		. . Screw, FLH100 6—32X7/16 (AP)	96906	MS24693—C27	4
1A3	6—3—3	. Power Supply No. 2	08742	RMV223B—2330—0450	1
		. . Screw, PNH—LKG (AP)	80205	NAS1635—08LL8	4
		. . Washer, Cres, Flat #8 (AP)	80205	MS15795—8074	
1A2	6—3—4	. Power Supply No. 1	80103	LFQ—27—1	1
		. .Screw, PNH—LKG (AP)	80205	NAS1635—08LL8	3
		. . Washer, Cres, Flat #8 (AP)	80205	MS15795—807	3

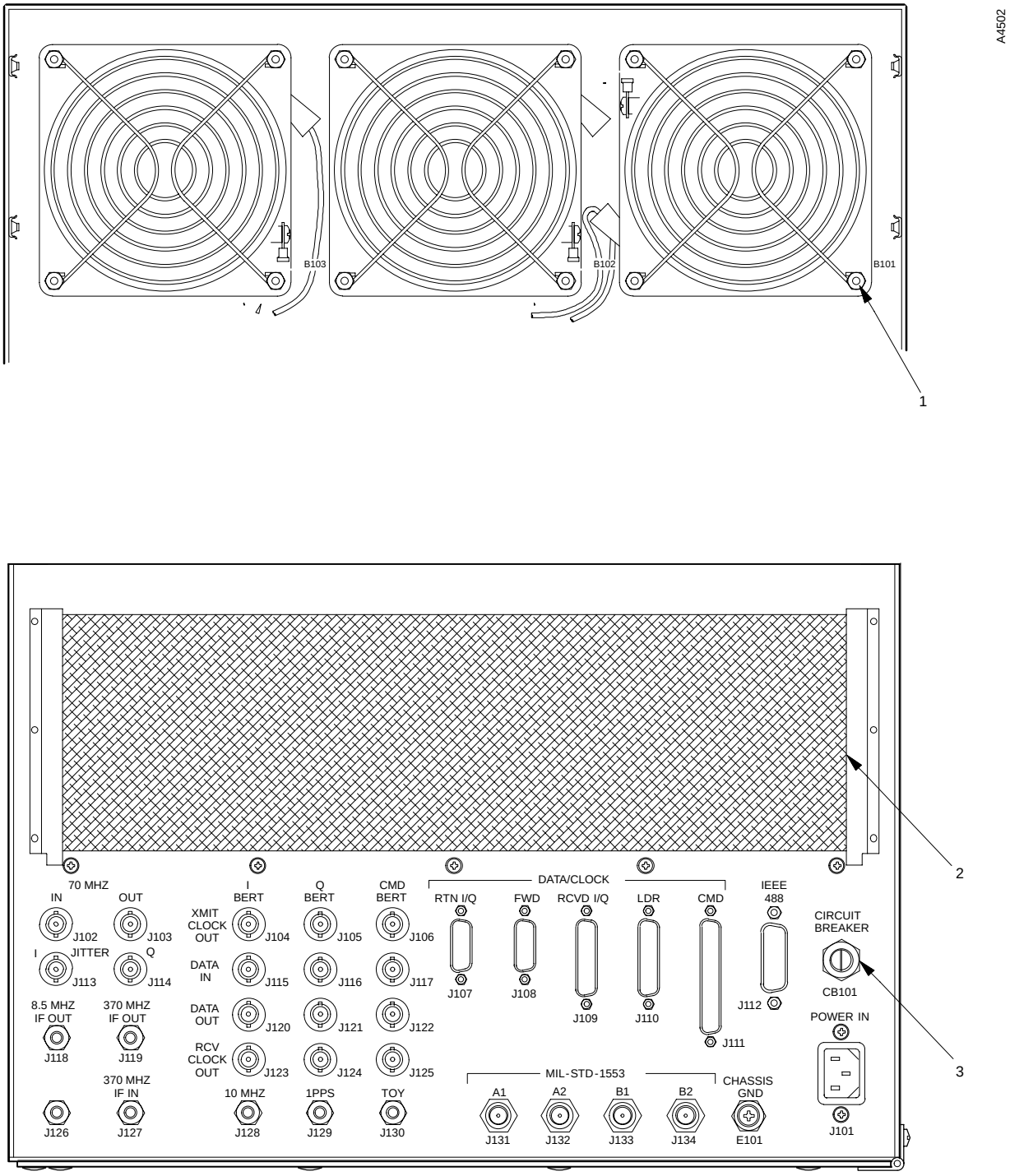


Figure 6—4. Test Modem (Rear View)

Table 6—6. Parts List, Test Modem (Rear View)					
REF. DES.	FIGURE/ IND. NO.	DESCRIPTION	CAGE/ FSCM	PART NUMBER	QTY
1	6—4	Test Modem (Rear View)	07421	7472500	REF
1A1B101 —B103	6—4—1	. Fan, Tubeaxial	25140	A47—B15A—15T3—000	3
		. . Grille, Metal (AP)	NMB	055015	3
		. . Screw, FLH 100 6—32X7/16 (AP)	96906	MS24693—C40	4
		. . Washer, Flat #6 0.312 O.D. (AP)	96906	MS15795—805	4
		. . Nut (AP)	96906	MS21045C06	
	6—4—2	. Filter, Air Cond	03102	3994—A	1
1A1— CB101	6—4—3	. Circuit Breaker	81349	MS25244—10	1

This Page Intentionally Left Blank

Section VII — Drawings

7—1 Introduction

This section refers to drawings necessary for maintenance technicians to understand the makeup and function of the power, control, and signal inputs/outputs to and from the TM major components and subcomponents. These drawings allow the technicians to trace the path of each input/output, make continuity checks, perform general and specific trouble analysis of inoperative or malfunctioning TM functions, and locate components within the TM. Refer to table 7-1 for a list of drawings necessary for Level 1 maintenance.

Table 7—1. List of Drawings

FIGURE NUMBER	TITLE	DRAWING NUMBER
	Test Modem Schematic Logic Diagram	EL7472501

This Page Intentionally Left Blank

Glossary

The following defines the abbreviations, acronyms, and mnemonics used in this manual.

ACQR	Acquisition processor PWA
ADPE	Automated data processing equipment
AGC	Automatic gain control
ASIC	Application—specific integrated circuit
AP	Attaching part
AR	As required
A/D	Analog to digital
BB	Baseband
BCD	Binary—coded decimal
BER	Bit error rate
BERT	Bit error rate tester
BIM	Bus interrupter module
BIT	Built—in test
BITE	BIT equipment
BPF	Band—pass filter
BPSK	Binary PSK
CAGE	Commercial and government entity
CC	Common carrier
Comcor2	2—bit fast acquisition correlator chip
CPU	Central processing unit
CTFS	Common time and frequency system
CW	Continuous wave
C/No	Carrier—to—noise—density ratio
DAC	Digital—to—analog converter
dB	Decibel
dBm	Decibel unit of power level with reference to a power of one milliwatt
DIS	Data interface system
DMA	Direct memory access
DMAC	DMA controller
DMDP	Demodulator processor PWA
DMSS	Demodulator/symbol synchronization PWA
DoD	Department of Defense
DPRAM	Dual ported RAM
DSP	Digital signal processor
D/A	Digital to analog
Eb/No	Bit energy—to—noise ratio
ECL	Emitter coupled logic
EIRP	Effective isotropic radiated power
EMI	Electromagnetic interference
EPROM	Electrically programmable ROM
ESD	Electrostatic discharge
EXCS	External clock synchronizer PWA
Exec	Executive program
FDU	Functional design unit
FFT	Fast fourier transform
FIR	Finite impulse response
FPCP	Floating—point coprocessor
FSCM	Federal supply code for manufacturers
GN	Ground network
GT	Ground terminal
HDR	High data rate
HMD	Hardware maintenance depot
HWCI	Hardware configuration item
I	Inphase
IC	Integrated circuit
IEC	Interstate Electronics Corporation
IF	Intermediate frequency
IPB	Illustrated parts breakdown
IR	Integrated receiver
IRIG	Inter—range instrumentation group
ISR	Interrupt service routine

I/D	Integrate/dump
I/O	Input/output
I488	IEEE—488 interface control PWA kbps kilobits per second
KSA	K—band single access
KSHR	K—band Shuttle return service
LBI	Local bus interface
LDR	Low data rate
LMT	Line maintenance technician
LO	Local oscillator
LPF	Lowpass filter
LRU	Line replaceable unit
LSB	Least significant bit
MA	Multiple access
Mbps	Megabits per second
MCP	Modem control processor PWA
MDP	Modulator/Doppler Predictor
MHz	Megahertz
MIPS	Megainstructions per second
Mmax	Maximum—time—to—repair
MPPC	Multiprotocol communications controller
MPL	Maintenance parts list
MSB	Most significant bit
MTG	Maintenance test group
MTTR	Mean—time—to—repair
MUX	Multiplexer
NASA	National Aeronautics and Space Administration
NASCOM	NASA communications network
NCO	Numerically controlled oscillator
NGT	NASA ground terminal
NRZ—L	Non—return to zero—level
NRZ—M	Non—return to zero—mark
NRZ—S	Non—return to zero—space
O&M	Operation and maintenance
OUTP	Output processor PWA
PE	Probability of error
PI/T	Parallel interface and timer
PLL	Phased—lock loop
PMMS	Performance measuring and monitoring system
PN	Pseudorandom—noise
PNP	PN processor PWA
PS	Power supply
PSK	Phase—shift keying
PTE	PMMS test equipment
p—p	Peak—to—peak
QPSK	Quadrature PSK
RAM	Random access memory
RF	Radio frequency
RFDC	RF Downconverter PWA
ROM	Read—only memory
RTA	Remote terminal address
RTC	Real—time clock
R/H	Run/halt
R/R	Removal/replacement
SN	Space network
SNR	Signal—to—noise ratio
SPS	Symbols per second
SQPSK	Staggered QPSK
SRAM	Static RAM
SSA	S—band single access
SSHR	S—band Shuttle return service
STDN	Spaceflight Tracking and Data Network
STGT	Second TDRSS Ground Terminal Tracking and Data Relay Satellite System
SYNTH	Synthesizer PWA
TB	Terminal board
TDIF	Test data interface PWA
TDRSS	Tracking and data relay satellite system
TIME	Timing generator PWA
TLC	Talk/listener/controller
TM	Test Modem

TMOD	Test modulator PWA
TMS	Texas Instruments TMS320C25 DSP
TN	TDRSS network
TOCC2	TDRS Operations Control Center No. 2
TOY	Time—of—year
TS	Tri—state
TTL	Transistor—transistor logic
UQPSK	Unbalanced QPSK
USS	User services subsystem
Vac	Voltage alternating current
VCO	Voltage controlled oscillator
VCXO	Voltage controlled crystal oscillator
Vdc	Voltage direct current
VME	Versa—Module European
VRTX	Versatile Real Time Executive

This Page Intentionally Left Blank